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SECTION 1

General Description and Specifications

1.0 GENERAL DESCRIPTION

IMS International manufactures microcomputer systems in two basic configurations: the 5000 and the 8000. They are differentiated by the size of their floppy disk drives. All 5000 systems use 5 1/4" floppy disk drives, and 8000 systems use 8" floppy disk drives. This manual examines the 5000 systems, describing each system and each board in detail.

There are two different IMS 5000 systems, the 5000SX and the 5000IS (Integrated System). Each uses the same boards, but they are in different enclosures.

IMS 5000SX systems are table top systems featuring an enclosure design which presents a pleasing modern appearance while retaining rugged construction. The 5000SX has provisions for three 5 1/4" drives, allowing any combination of floppy drives and Winchesters with up to two Winchester drives. Nine unused slots are available for system expansion. If the system has a Winchester drive, the Winchester controller board occupies one of these free slots.

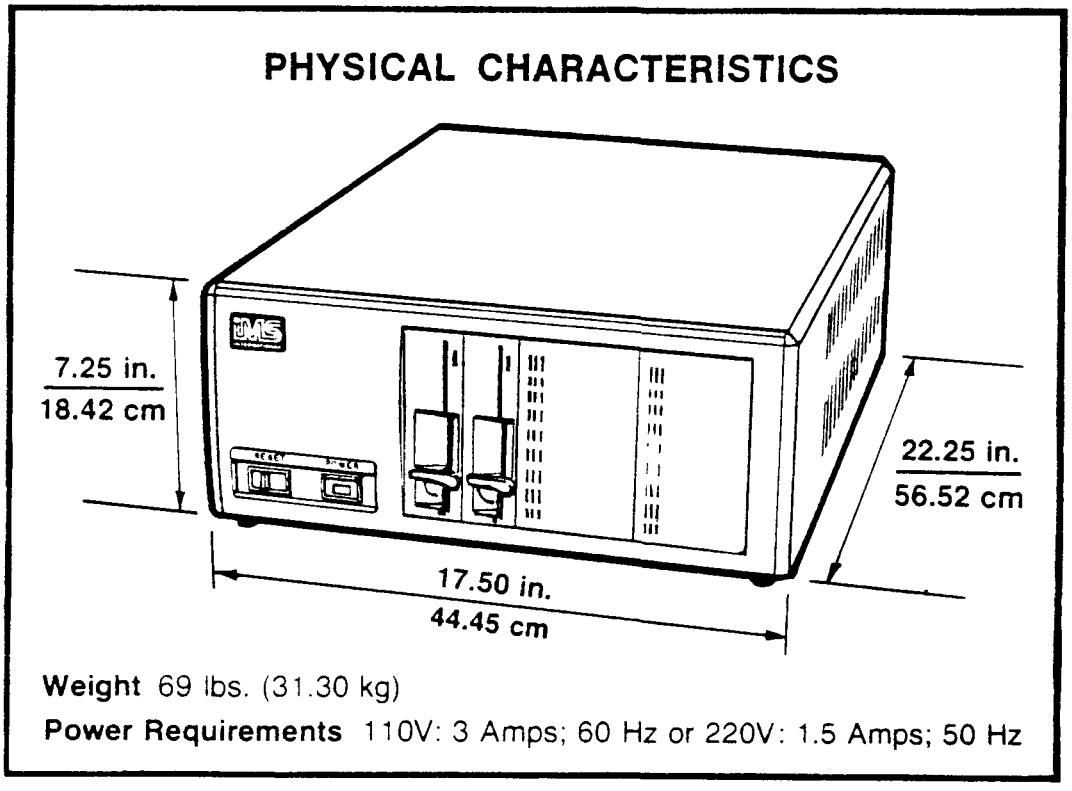


Figure 1-1
5000SX Microcomputer System and Dimensions

5000IS systems are integrated systems built into one compact unit. Each system has a CRT and a detachable keyboard. There is room for three drives, usually one Winchester and two half-width floppy disk drives. Five card slots are available for future system expansion. The Winchester controller board, if used, occupies one slot.

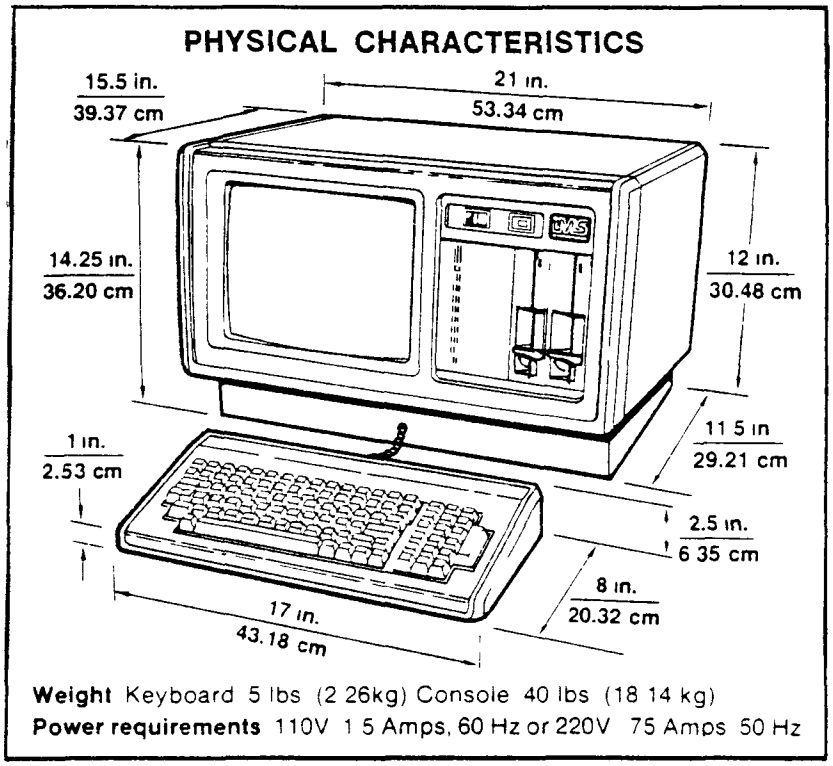


Figure 1-2

5000 IS Microcomputer System and Dimensions

All standard 8 bit 5000 systems contain the following features:

- 4 MHz Z80A Processor
- 64K Dynamic RAM with Parity
- Selectable Baud Rate up to 19.2 KB with full modem control
- Floppy Disk Drive Subsystem
- Real Time Calendar/Clock with Battery Backup
- S-100 Motherboard
- Two year IMS Warranty

The differences between the 8 bit 5000IS and the 5000SX are listed below.

8-bit 5000 IS	8-bit 5000SX
8 slot motherboard	12 slot motherboard
high resoution CRT	
detached keyboard	

Two add-on options are available for all IMS systems; the Multi-Processor Unit and the Cartridge Tape System.

The Multi-Processor Unit [MPU] is a board which converts a single user system into a multi-processing environment. The board contains a Z-80A microprocessor, 64 Kbytes of dynamic RAM with parity, four programmable interval timers, a 2 Kbyte boot EPROM, and a dual channel synchronous/asynchronous communication controller with full modem support, auto answer and auto dial. The MPU interfaces to the host CPU as an I/O device on the S-100 bus. Up to sixteen MPUs may be used in a single system. This board provides each user the performance of a dedicated processor while allowing access to a common data base.

The cartridge tape system serves as a start/stop backup memory for the high performance Winchester, and can also be used as a memory subsystem for data files and programs as would be required in a normal data processing environment. The tape unit uses the standard ANSI cartridge (DC 300XL). The capacity of each cartridge varies depending on the format selected. The tape cartridge unit is mounted in a stand-alone enclosure.

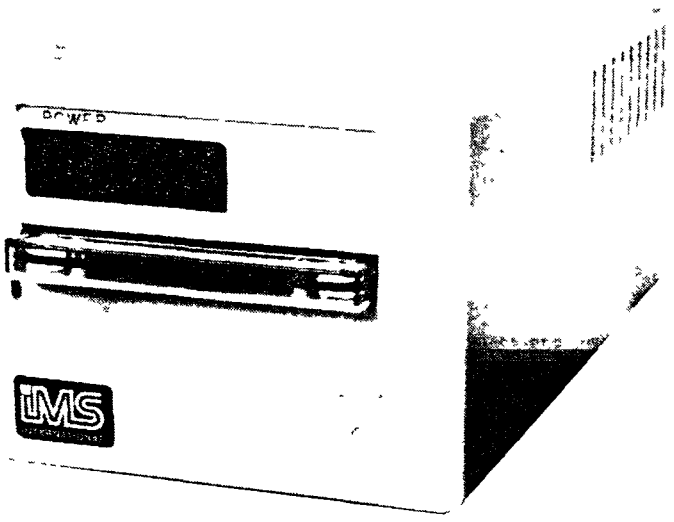


Figure 1-3
Cartridge Tape Stand Alone Unit

Another option on IMS systems is the selection of the floppy disk drive size. There are two types of 5" floppy disk drives available from IMS, the double density (48 tracks per inch) and the quad density (96 tracks per inch) half-width drives.

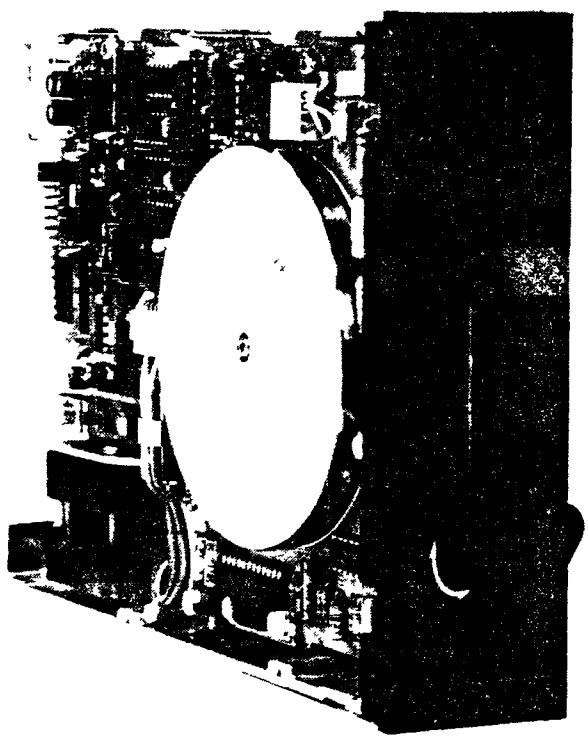


Figure 1-4
5 ¼" Floppy Disk Drive

SECTION 2

Theory of Operation

2.0 SYSTEM BLOCK DIAGRAM

The block diagrams for the 5000IS and the 5000SX are illustrated below. Each IMS system contains a Central Processing Unit (CPU), Memory, Input and Output capability and some type of memory storage (floppy disks or Winchester disks). In addition, the system can be expanded by adding a tape cartridge unit and/or adding multi-processing capabilties with the MPU board.

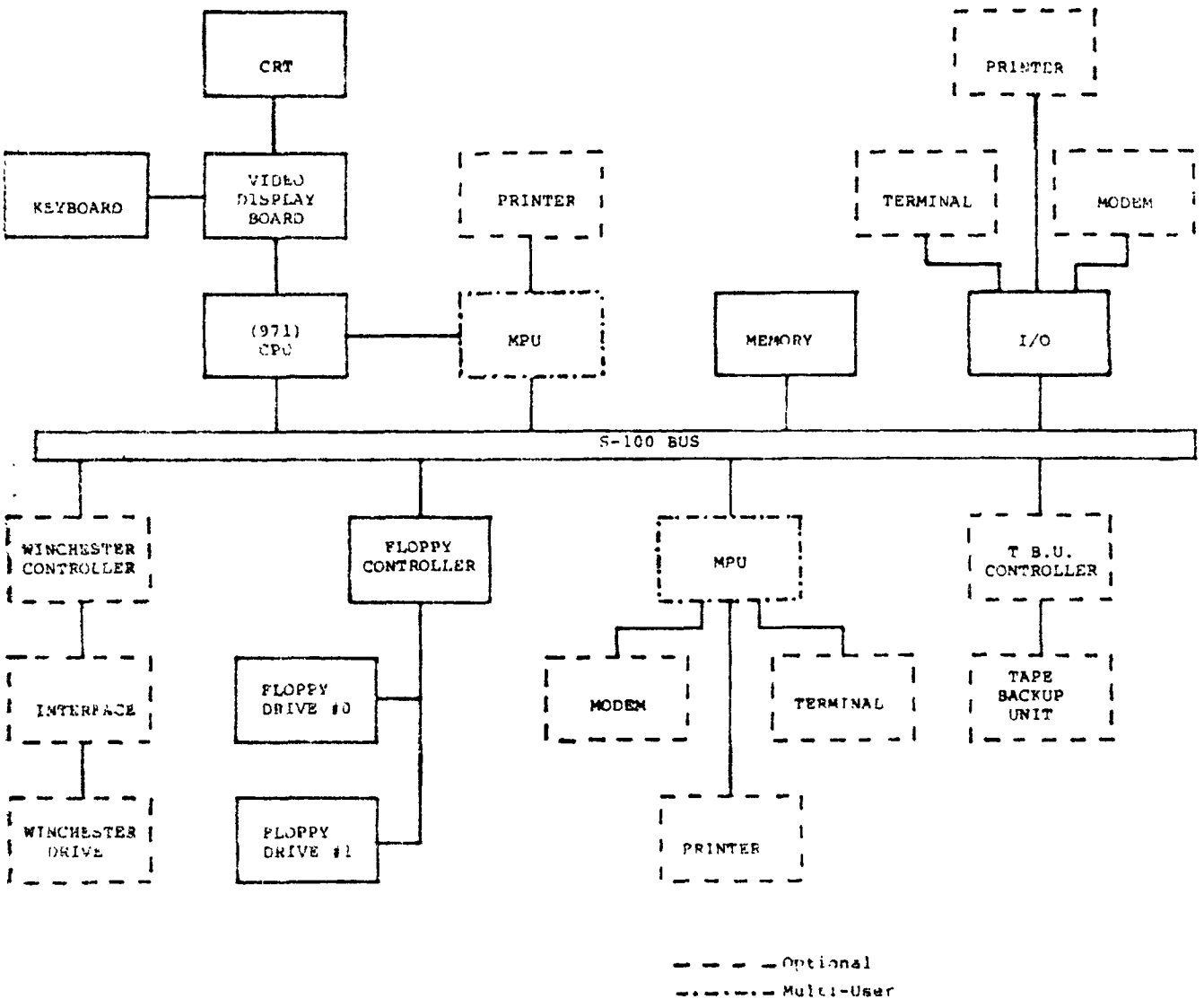


Figure 2-0
5000IS Block Diagram

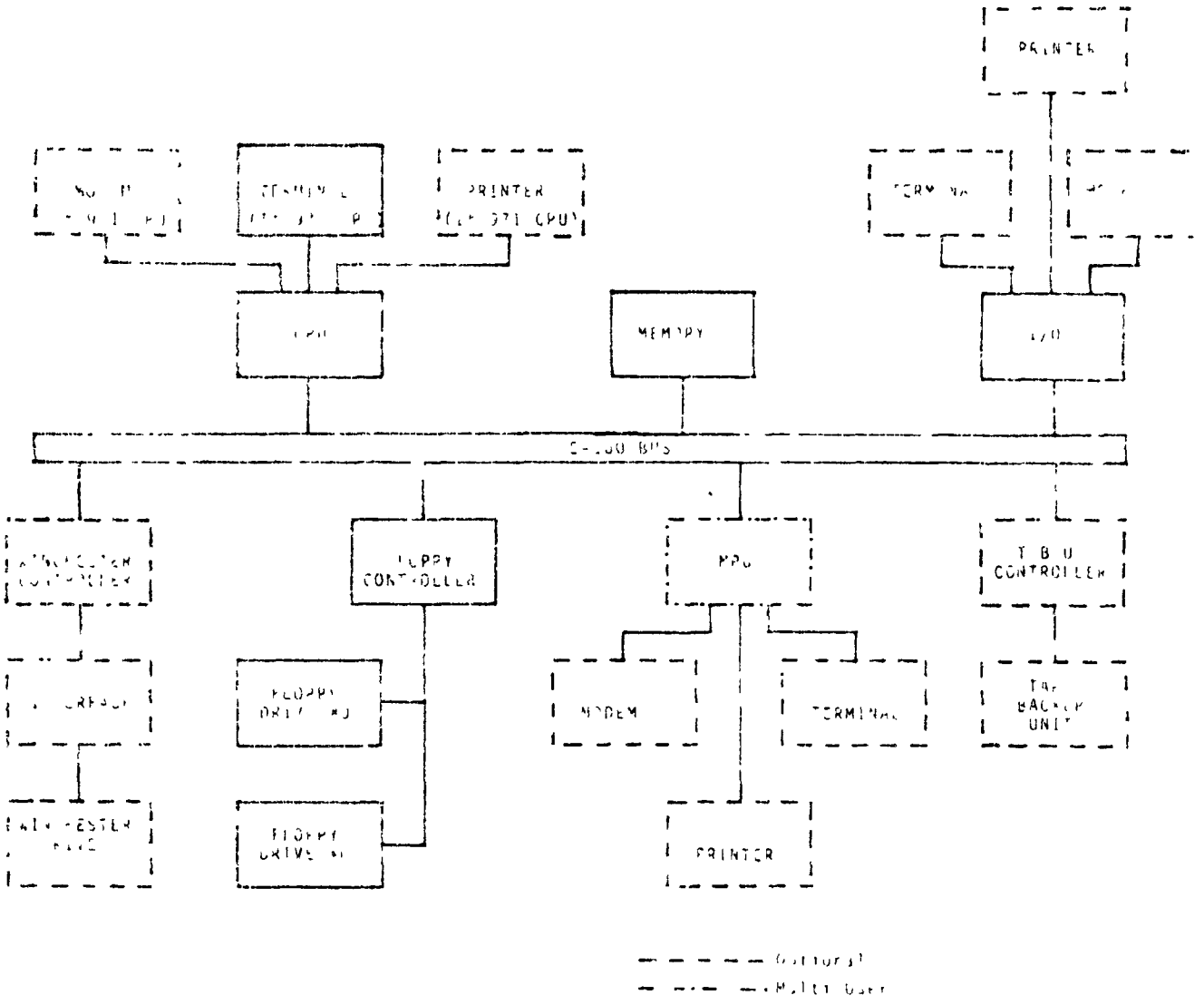


Figure 2-1
5000SX Block Diagram

In the system block diagrams, each block connected to the S-100 bus represents an IMS circuit board. The actual bus is contained in the motherboard.

Numbers and abbreviations are used to identify each board.

Board Number	Abbreviation	Description
451	CPU-A	Z-80 Processor Board
645	CPU-B	Z-80 Processor Board
971	ZPU/IO	Z-80 Processor Board
881	8088ZPU	8088 Processor Board (16 bit)
465	64DRAM	Memory-64K
961	256DRAM	Memory-256K (for 16 bit systems)
444	SPIO	Input/Output (2 serial, 3 8-bit parallel ports)
631	SPIO-B	Input/Output (2 serial, 3 8-bit parallel ports)
480	4SIO	Input/Output (4 serial ports)
740	MPU	Z-80 Multiprocessor Board
861	MPU	Z-80 Multiprocessor Board
431	FDC	5" Floppy Disk Drive Controller Board
930	FDC	5" or 8" Floppy Drive Controller Board
820	HDC	Winchester Disk Controller Board
662	VDB	Video Display Board (5000IS only)

The last digit in the board number indicates the revision level. For example, a 444 I/O board is the same as a 440 I/O board except for a few minor changes.

Different combinations of boards may be used to make up a system. The most common are listed below.

CPU	I/O	Memory
451	444	465
645	631	465
645	480	465
--971--		465

2.1 MOTHERBOARD

The motherboard is the board which holds all the other boards. It provides power and communication signals. The protocol used for the signals is based on the S-100/IEEE696 standard. IMS motherboards are not slot dependent; any card can go into any slot. Generally, the boards are spread out to provide ventilation between them. The only reason you might put a card in one place and not another is the cabling considerations; other than that, you may move a card anywhere you want. IMS 5000 systems have two sizes of motherboards; the 5000IS motherboard has 8 slots and the 5000SX has 12.

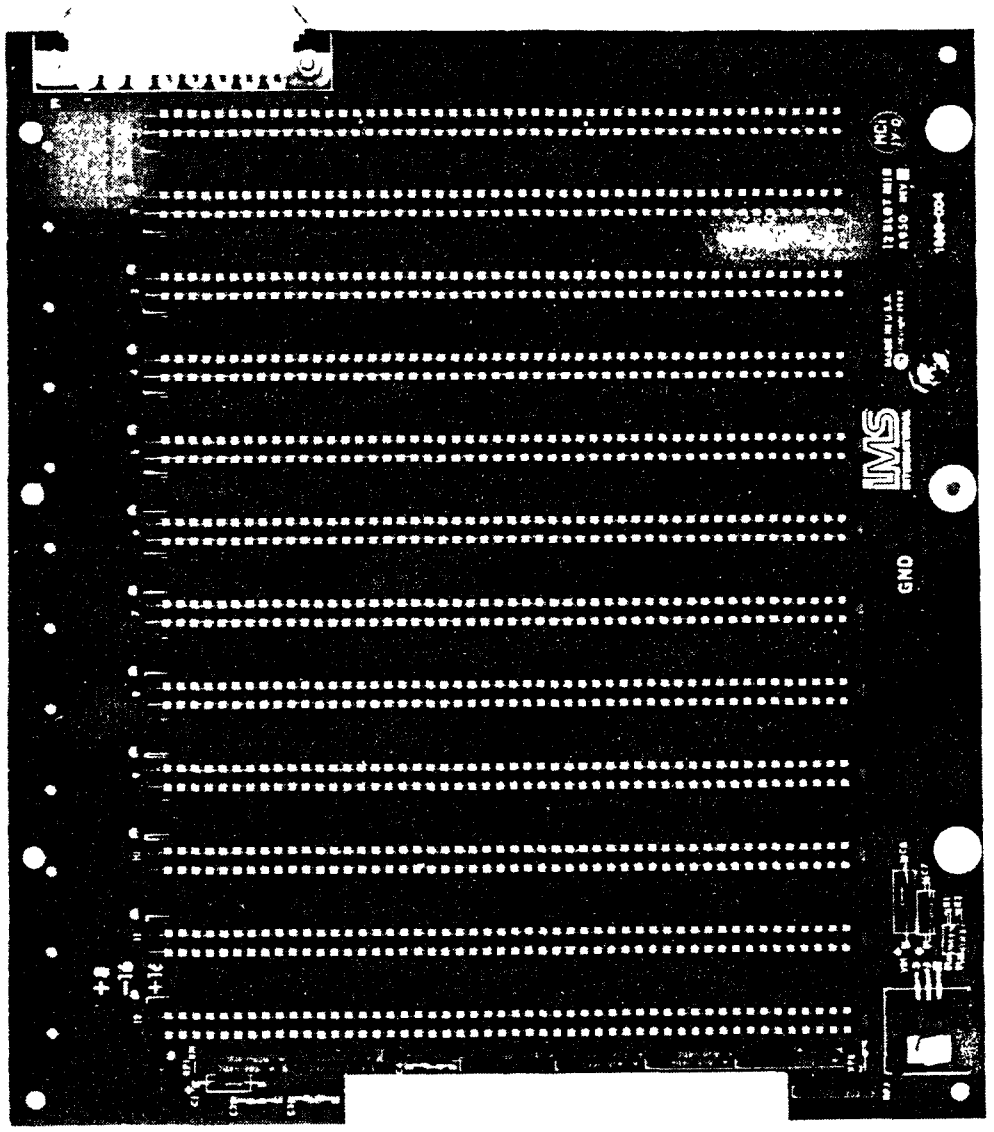


Figure 2-2
Twelve Slot Motherboard

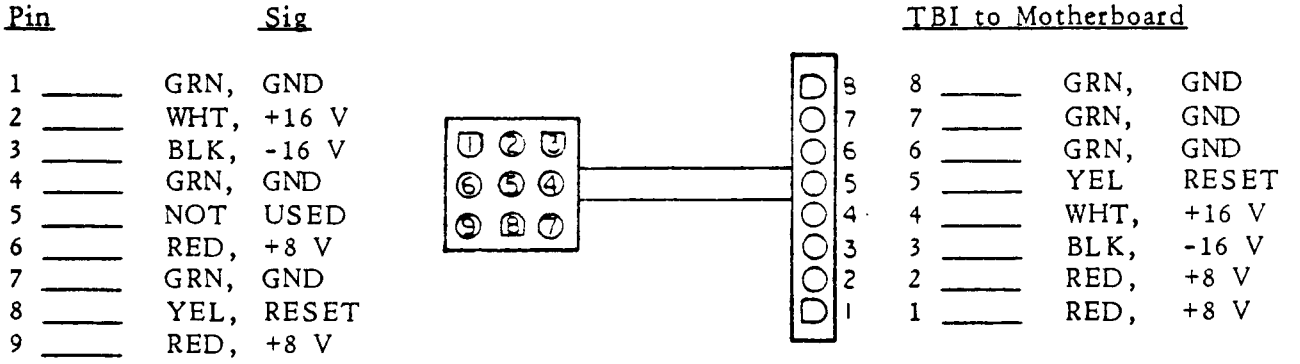


Figure 2-3
DC Power Supply to Motherboard Connection

2.2 BOARD SHUNTING

Each device in the microcomputer which needs to directly communicate with the Central Processing Unit (CPU) is assigned a unique number which is called its I/O address. The CPU can communicate exclusively with one device by using certain instructions which broadcast a specific address over the bus. In IMS systems, selection is done by comparison. Each device looks at the address on the bus and compares it to its address; if they are the same, then that device is selected.

Each board (except the CPU board) has a set of shunts on it to specify its address. Each shunt assigns a specific value to a certain address bit. If the shunt is off, that address bit is assigned a '1' value; if the shunt is on, the address bit is equal to a '0'.

The MPU (740) board, for example, takes up four I/O address locations on the bus. The boards normally occupy I/O addresses 40H to 5FH and E0H to FFH. These locations enable us to include up to 16 boards in the system. Look at the shunt positions JE and the value of each shunt:

JE	Value with Shunt OFF (and the rest ON)	Value with Shunt ON
A7 o o	80H	00H
A6 o o	40H	00H
A5 o o	20H	00H
A4 o o	10H	00H
A3 o o	08H	00H
A2 o o	04H	00H

The values are determined by the address bit they are being compared to. If we look at JE as a binary number, we have:

A7, A6, A5, A4, A3, A2 ⟶ XXXX XX00B⟶ XXH

By setting the bits either high or low, we define our address. A1 and A0 are both set to 0 since the board is addressed in units of 4H.

Examples:

Shunts (S=ON, U=OFF)						Binary Value		Hex Address
A7,	A6,	A5,	A4,	A3,	A2	--> XXXX	XX00	--> XXH
S,	U,	S,	S,	S,	S	0100	0000	40
S,	U,	S,	U,	U,	U	0101	1100	5C
U,	U,	U,	S,	S,	U	1110	0100	E4
U,	U,	U,	S,	U,	S	1111	1000	F8

I/O Addresses Used by IMS Boards

00-0FH	Memory boards
00	First memory board
01-03	Additional memory boards
06,07	881 Processor board
10H-1FH	44x I/O board
	645 Processor board
	971 Processor board
20H-3FH	971 Processor board
	631 I/O board
	480 I/O board
40H-5FH	First 8 MPU boards (740 or 861)
60H-7FH	645 Processor board
	971 Processor board
	881 Processor board
80-8FH	401 8" Floppy Disk Drive Controller
	930 8" Floppy Disk Drive Controller
90H-9FH	Currently unused
A0H-A7H	820-5 5" Winchester Controller
A8H-AFH	820-8 8" Winchester Controller
B0H-BFH	Reserved for customer use
C0H-CFH	431 5" Floppy Disk Drive Controller
	930 5" Floppy Disk Drive Controller
D0H-DFH	Tape Back-up Unit
E0H-FFH	Additional MPU boards (740 or 861)
	or second 480 I/O board

Interrupt Vectors

IMS peripherals have the capability of being interrupt driven. This means that the controller will send a request for service directly to the processor instead of waiting for a polling routine to service it. The processor supports 8 interrupt levels, Vector Interrupts 0 to 7, with VI0 having the highest priority. The boards can be shunted to interrupt the processor at a certain level. The current levels are listed below with their function and the boards that use them.

Vector Interrupt	Function
VI0	Reserved by CP/M
VI1*	Relative Time Clock (444 and 645 boards) Time of Day CLock (645 board)
VI2**	Memory Parity Error (465 board)
VI3*	Serial Communications (444, 480, 631 boards)
VI4	Hard Disk (820 board)
VI5	Floppy Disk (401, 431, 930 boards)
VI6	Reserved for Customer Use
VI7	Reserved by CP/M

*not used by CP/M operating system.
**not used by TurboDOS

2.3 POWER SUPPLY

The IMS 5000IS and 5000SX use a switching power supply with the following specifications:

Input: 100-130 V (60Hz) at 3 A maximum, or
200-260 V (50Hz) at 1.5 A maximum.

Output Voltage	Output Current
+5 V	3A
+12 V	7A
+8.5 V	10A
+16 V	4A
-16 V	0.5A

Note: Maximum load is 200 W total.

Figure 2-4
Power Supply Specifications

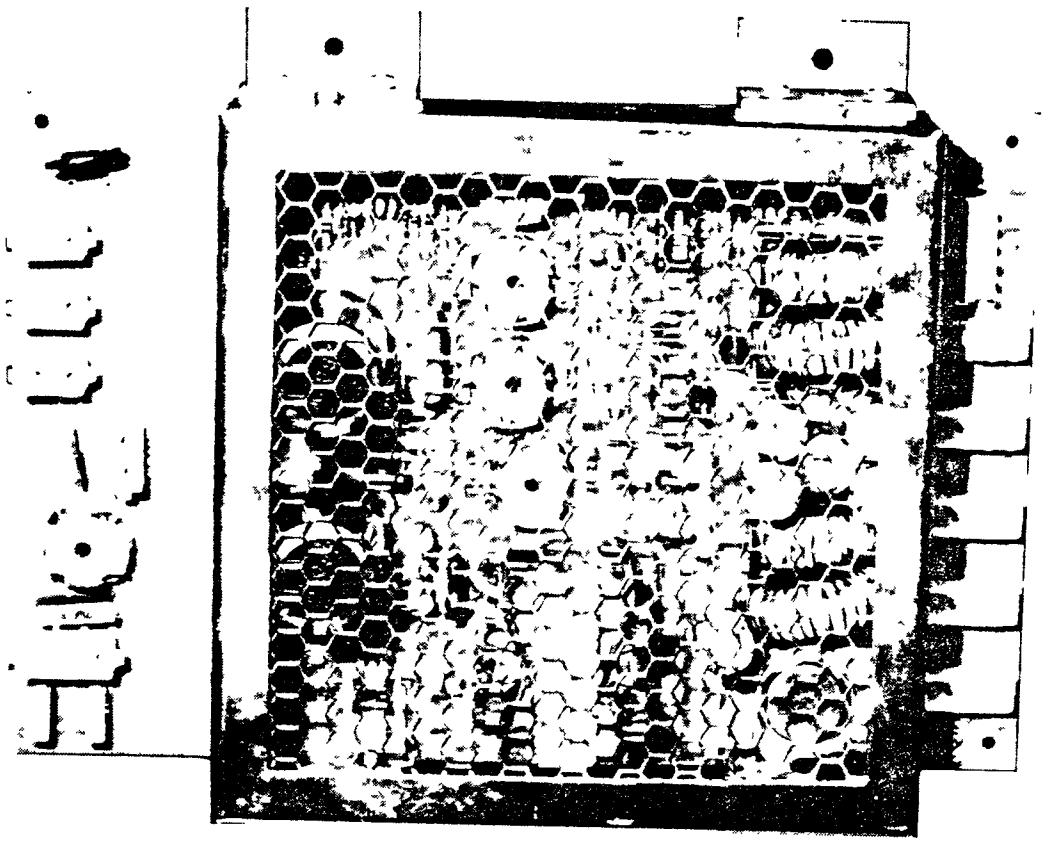


Figure 2-5
Power Supply

2.4 CENTRAL PROCESSOR BOARDS

2.4.1 MODEL 451 - Z80 PROCESSOR BOARD

GENERAL DESCRIPTION

The Model 451 Processor is the Central Processing Unit (CPU) of the IMS International Series 5000 and 8000 Computer Systems. The Model 451 provides control for the system. The 451 uses a Z-80 microprocessor for control. The Z-80 has priority vectored interrupts and the ability to address 256 I/O addresses, as well as a central processing unit.

The Model 451 processor consists of a single printed circuit board that can occupy any slot in the Series 5000 or 8000 computer systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 bus system.

The 451 processor board consists of the following functional divisions:

- Z-80 8-bit Microprocessor Device (CPU)
- Priority Vectored Interrupt Circuitry
- S-100 Bus Interface

SPECIFICATIONS

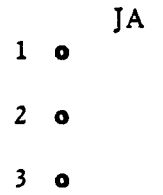
• Word Size:	Address	16 bits
•	Data	8 bits
• Directly Addressable Memory:		64Kbytes
• Clock Frequency:		4 MHz
• Circuit Board Dimensions:		5.25" x 10"
• Power Requirements:		+8V @ 700 ma

CONFIGURING THE 451 Z-80 CPU BOARD

Legend

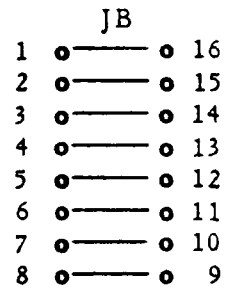
Wait State Select (Location JA)

The position of the shunt at JA indicates the number of states that the processor waits after a memory read operation.



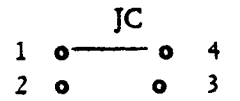
No shunts = No memory wait state (normal)
Shunt JA 1-2 = One wait state
Shunt JA 2-3 = Two wait states

Power On Address Select (Location JB)



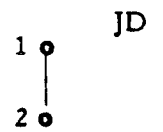
The shunt at JB indicates the address that the processor jumps to when the system is powered up. A shunt on a bit assigns a 0 value to that bit; a bit with no shunt is assigned a '1' value. So with all the shunts on, the power-on address is 0000H. With all the shunts off, the power-on address is FF00H. This location is normally etched for an address of 0000.

CPU Clock Select (Location JC)



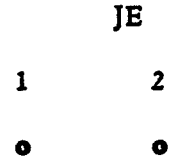
This shunt is etched to provide the Z-80A microprocessor with a 4MHz clock.

Address Mirror Select (Location JD)



When this location is shunted, the Address Mirror duplicates the I/O address onto the upper 8 address lines.

MWRITE+ ENABLE (Location JE)



A shunt on location JE allows the MWRITE+ signal (indicating a write to memory) to go out onto the bus. Normally, this location is unshunted.

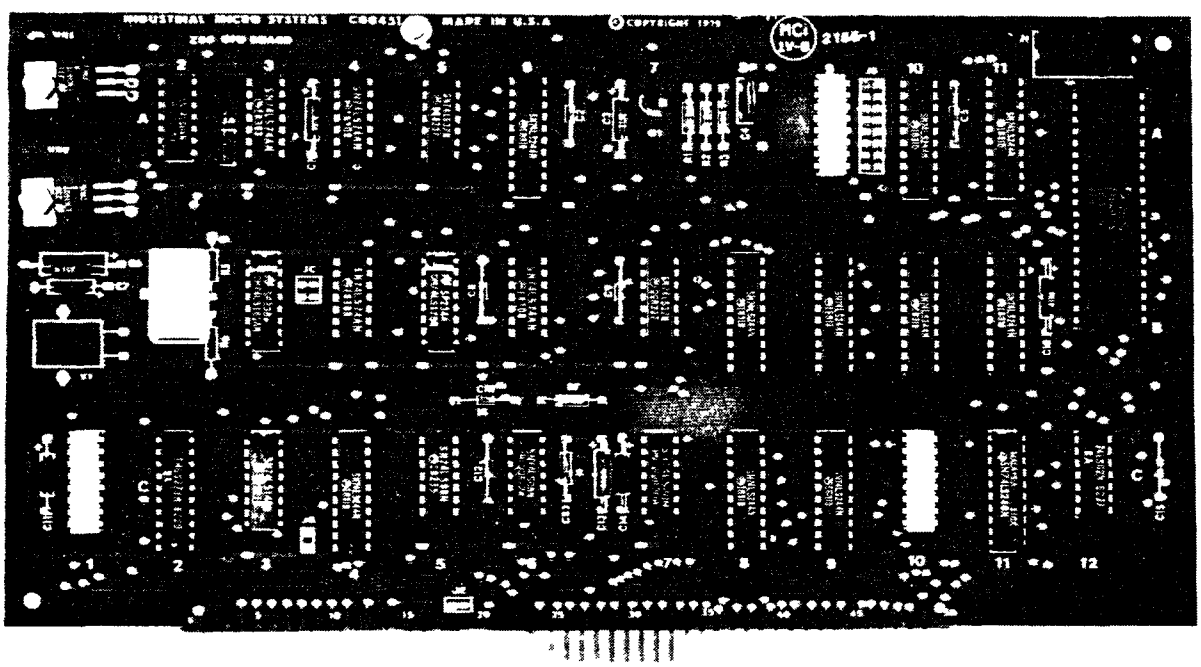


Figure 2-6
Model 451 CPU Board

2.4.2 MODEL 645 - Z80 PROCESSOR BOARD

GENERAL DESCRIPTION

The Model 645 Processor Board is the Central Processing Unit (CPU) of the IMS INTERNATIONAL Series 5000 and 8000 Computer Systems. The Model 645 provides control for the system.

The 645 uses a Z-80 microprocessor for control of the system. The Z-80, besides being the central processing unit, has priority vectored interrupts and the ability to address 256 I/O ports.

A chronograph function is provided by the 58167 real-time clock. The circuit includes addressable counters for tenths of seconds through months and a write only register for leap year calculation. A relative time clock function is also available using an 8253 programmable interval timer.

The Model 645 processor consists of a single Printed Circuit Board. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus System.

The 645 Processor Board consists of the following function divisions:

- Z-80 8-bit Microprocessor (CPU)
- Priority Vectored Interrupt Circuitry
- Programmable Interval Timer
- Real-Time Clock
- 2048 by 8-bit EPROM

SPECIFICATIONS

• Word Size:	Address	16 bits
	Data	8 bits
• On-Board ROM:		2Kbytes standard. (May be shunt selected to use 4 Kbyte EPROMS)
• Directly Addressable Memory:		64Kbytes
• Clock Frequency:		4 MHz
• Circuit Board Dimensions:		5.25"x 10"
• Power Requirements:		+8V @ 900 ma

I/O DEVICE ADDRESSES USED BY THE 645 CPU BOARD

14H-17H	8253 Programmable Interval Timer
14H	8253A Counter #0 R/W
15H	8253A Counter #1 R/W
16H	8253A Counter #2 R/W
17H	8253A Write Mode word
18H	2716 or 2732 EPROM Enable and 8253 RTC Interrupt Mask
bit 0	2716 EPROM Disabled when bit 0=1
bit 1	8253A RTC Interrupt enabled when bit 1=1. NOTE: While EPROM is enabled, the first 4 Kbytes of memory are occupied whether the actual EPROM is 2 or 4 Kbytes.
19H	8253A RTC F/F Reset
1BH	58167 CLK Interrupt Mask
bit 0	58167 CLK Interrupt enabled when bit 0=1.
60H-7FH	58167 Clock Internal Register Select
60H	R/W Counter - Thousandths of Seconds
61H	R/W Counter - Hundredths and tenths of seconds
62H	R/W Counter - Seconds
63H	R/W Counter - Minutes
64H	R/W Counter - Hours
65H	R/W Counter - Day of the Week
66H	R/W Counter - Day of the Month
67H	R/W Counter - Months
68H	R/W Latches - Thousandths of Seconds
69H	R/W Latches - Hundredths and Tenths of Seconds
6AH	R/W Latches - Seconds
6BH	R/W Latches - Minutes
6CH	R/W Latches - Hours
6DH	R/W Latches - Day of the Week
6EH	R/W Latches - Day of the Month
6FH	R/W Latches - Months
70H	R/O Interrupt Status Register
71H	W/O Interrupt Control Register
72H	W/O Counter Reset
73H	W/O Latch Reset
74H	R/O Status Bit
75H	W/O "GO" Command
76H	W/O Standby Interrupt
7FH	Test Mode

CONFIGURING THE 645 CPU BOARD

Wait State Selection

The "WAIT" shunt indicates the number of wait states the CPU waits after a memory access. It is presently etched for no wait states.

ROM Location Selection

The "ROM" shunt is etched to indicate that the Initial Program Loader (IPL) boot ROM is located on the 645 board. If this connection is cut, the system assumes that the IPL is on the I/O board.

EPROM Type Selection

The "16/32" shunt indicates the type of EPROM used. The "16" side is etched to indicate the use of a 2716 2Kbyte EPROM. If this connection was cut and the "32" side shunted, it indicates that a 2732 4Kbyte EPROM is being used.

Interrupt Level Selection

The "VI1, VI7" shunt indicates the interrupt level for the real-time clock. This is normally etched for level VI1.

MODEL 645 Z80 PROCESSOR BOARD

Legend

1. VR1, VR2 - + 5 volt regulator.
2. WAIT - Etched for no wait states.
3. ROM - Normally etched for IPL boot PROM on CPU board.
4. IPL (Initial Program Loader) Boot PROM.
5. 16/32 EPROM Type Shunt - The "16" side is normally etched for a 2716 EPROM.
6. 3V BATTERY (B1) - for Clock/Calendar. The battery maintains time while the system is powered down.
7. VI1, VI7 - Clock interrupt. Normally etched for VI1.
8. MWRT - Normally not etched. Puts MWRITE+ signal on S100 bus when shunted.

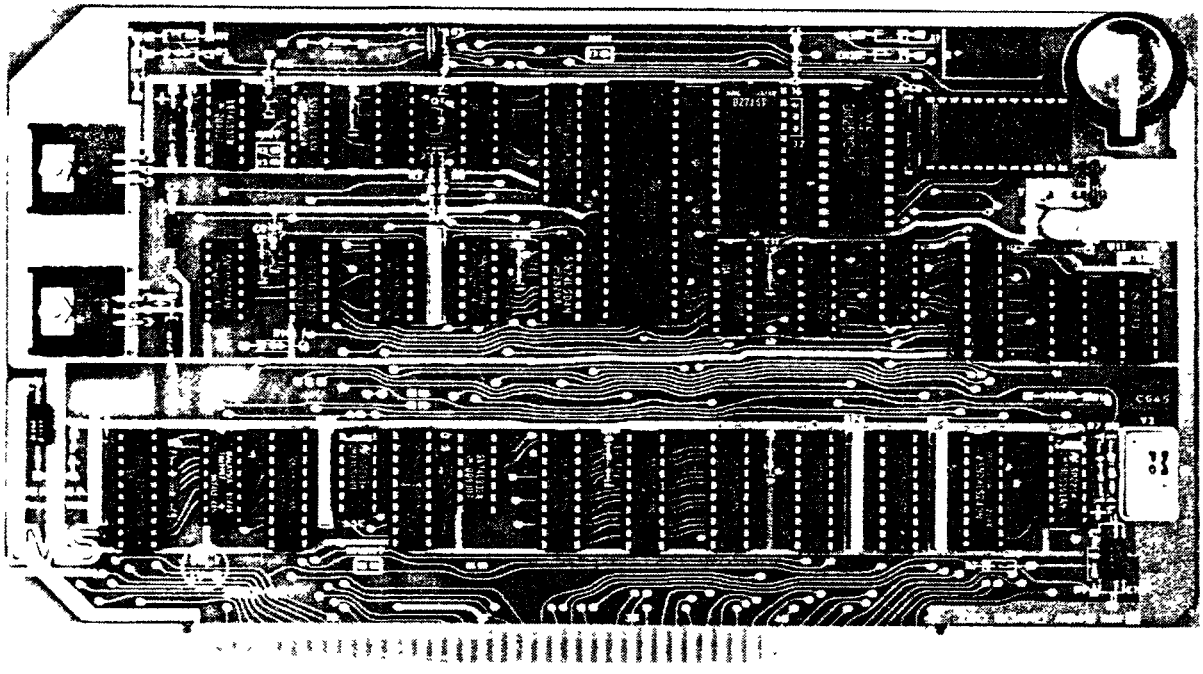


Figure 2-7
Model 645 Z80 Processor Board

2.4.3 MODEL 971 - Z80 PROCESSOR BOARD

GENERAL DESCRIPTION

The 971 Processor Board is the Central Processing Unit (CPU) of IMS International systems. This board controls the rest of the system.

The heart of the 971 board is the Z-80A microprocessor. The Z-80 has 158 instructions with a 1 msec instruction cycle time. It has a 16-bit address bus, which means it can address 64 Kbytes of memory directly, and an 8-bit data bus. It can address 256 bi-directional I/O ports and has priority vectored interrupts.

Interrupts are used so a device can signal the CPU for attention, instead of waiting for the CPU to poll it. There are eight different levels of interrupts, each with a different priority. They are labeled Vector Interrupt 1 to Vector Interrupt 7 (VI0-VI7); VI0 has the highest priority.

The 971 has a real-time clock in the form of the 58167 integrated circuit. This chip has addressable real-time counters which count from tenths of seconds to months.

The 971 board has two serial ports which are connected, via cables, to the I/O panel on the back of the machine. These ports are controlled by the 8250 Asynchronous Communications Controller. This chip converts the serial data from the port to parallel data for the system; it also converts parallel data to serial data to be output to the port. These ports use the RS-232 protocol; for some connections, wires may need to be exchanged for proper operation.

This board also contains the IMS Intial Program Loader (IPL) boot EPROM. The program in this EPROM is used when the computer is first turned on or reset.

The Model 971 processor consists of a single Printed Circuit Board that occupies one slot in the Series 5000 or 8000 Computer Systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 bus.

The 971 Processor Board consists of the following function divisions.

- Z-80A 8-bit Microprocessor (CPU)
- Priority Vectored Interrupt Circuitry
- Two Serial RS-232C Ports
- Real-Time Clock
- 2K/4K/8K by 8-bit EPROM

SPECIFICATIONS

• Word Size:	Address	16 bits
	Data	8 bits
• On-Board ROM:		2/4/8 Kbytes
• Directly Addressable Memory:		64Kbytes
• Clock Frequency:		4 MHz
• Circuit Board Dimensions:		5.25"x 10"
• Power Requirements:		+8V @ 900 ma
		+16V @ 50 ma
		-16V @ 50 ma

CONNECTIONS

The 971 connects to the S-100 bus through the gold plated pins on the bottom edge of the board. In addition, there are four connectors on the top edge of the board. In a 5000SX, J1 and J2 (the two wide connectors) are connected to channels 1 and 2, respectively, on the I/O panel on the back of the system. In a 5000IS, J2 is connected to the serial printer port on the back of the machine, J3 (a smaller connector) is connected to connector J5 on the 662 Video Display board, and J4 is connected to connector J3 on the 861 board if you have a multi-user system.

The cable signals and connections for connecting data terminal equipment to the 971 are shown below. This connection is made via the I/O panel on the back of the machine.

Signal Name	RS-232C Circuit	971 J1 or J2 Pin		DTE Connector Pin
Transmit Data	BA	3	------	2
Receive Data	BB	5	-----	3
Request to Send	CA	7	------	4
Clear to Send	CB	9	------	5
Data Set Ready	CC	11	------	6
Signal Ground	AB	13	------	7
Data Terminal Ready	CD	14	------	20
Data Carrier Detect	CF	15	------	8
Ring Indicator	CE	18	------	2

Model 971 Serial Port to RS-232C Connector Cable

I/O DEVICE ADDRESSES FOR THE 971 CPU BOARD

18H	2716/32/64 EPROM Enable
bit 0	EPROM is disabled when bit 0=1.
1BH	58167 CLK Interrupt Mask
bit 0	58167 CLK Interrupt is enabled when bit 0=1.
20H-27H	Port 0 8250 ACE Internal Register Select
20H	Read Receive buffer/ Write Holding Register (DLAB=0)
20H	Write Divisor Latch least significant byte (DLAB=1)
21H	R/W Interrupt Enable Register (DLAB=0)
21H	Write Divisor Latch most significant byte
22H	Read Interrupt Identification Register
23H	R/W Line Control Register
24H	R/W Modem Control Register
25H	R/W Line Status Register
26H	R/W Modem Status Register
27H	Nothing
28H-2FH	Port 1 8250 ACE Internal Register Select
28H	Read Receive buffer/ Write Holding Register (DLAB=0)
28H	Write Divisor Latch least significant byte (DLAB=1)
29H	R/W Interrupt Enable Register (DLAB=0)
29H	Write Divisor Latch most significant byte
2AH	Read Interrupt Identification Register
2BH	R/W Line Control Register
2CH	R/W Modem Control Register
2DH	R/W Line Status Register
2EH	R/W Modem Status Register
2FH	Nothing
60H-7FH	58167 Clock Internal Register Select
60H	R/W Counter - Thousandths of Seconds
61H	R/W Counter - Hundredths and Tenths of Seconds
62H	R/W Counter - Seconds
63H	R/W Counter - Minutes
64H	R/W Counter - Hours
65H	R/W Counter - Day of the Week
66H	R/W Counter - Day of the Month
67H	R/W Counter - Month
68H	R/W Latches - Thousandths of Seconds
69H	R/W Latches - Hundredths and Tenths of Seconds
6AH	R/W Latches - Seconds
6BH	R/W Latches - Minutes
6CH	R/W Latches - Hours
6DH	R/W Latches - Day of the Week
6EH	R/W Latches - Day of the Month
6FH	R/W Latches - Month
70H	R/O Interrupt Status Register
71H	W/O Interrupt Control Register
72H	W/O Counter Reset
73H	W/O Latch Reset
74H	R/O Status Bit
75H	W/O "GO" Command
76H	W/O Standby Interrupt
7FH	Test Mode

CONFIGURING THE 971

Wait State Select (JA)

This shunt indicates the number of states that the CPU waits after a memory read. Normally, this is etched so there are no wait states. The other shunt location provides for one wait state.

EPROM Type Selection (JC)

This shunt is used for different types of EPROMs. If the 971 has a 2716 (2K) EPROM, the lower pair is etched. If the 971 has a 2732 (4K) or a 2764 (8K) EPROM, the upper pair is connected.

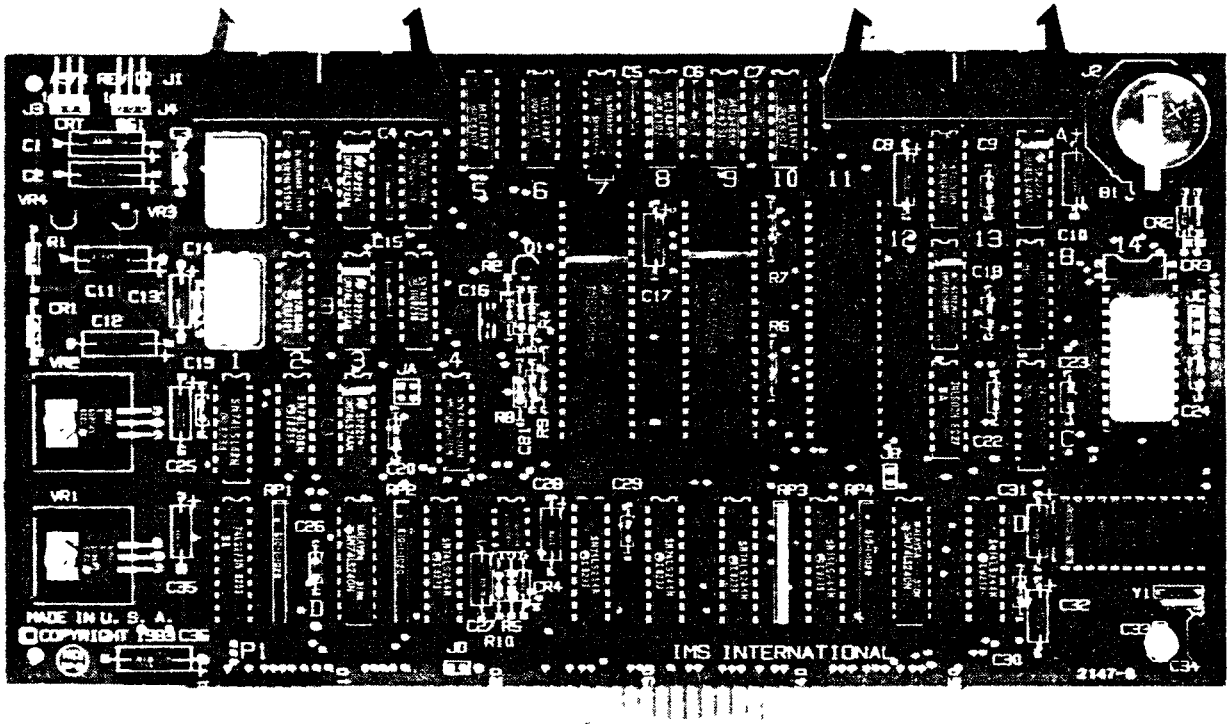


Figure 2-8
Model 971 Z-80 Processor Board

2.4.4 MODEL 881 - 8088 PROCESSOR BOARD

GENERAL DESCRIPTION

The 881 Processor Board is the Central Processing Unit (CPU) of the IMS International 16-bit systems. The main part of this board is the 8088 microprocessor. The 8088 has an 8-bit data bus interface with a 16-bit internal architecture. It has 20 address lines, allowing it to directly address up to 1 megabyte of memory. It also has priority vectored interrupt capability. There are eight levels of vectored interrupts, VI0 to VI7; VI0 has the highest priority.

The 881 board has a real-time clock circuit (the 58167 chip), which has counters for tenths of seconds to months.

The Initial Program Loader (IPL) EPROM is located on the 881 board. The program in this EPROM is executed when the system is powered up or reset.

There is also an option for an 8087 Numeric Data Processor. This increases the processor's capability for numerical calculations.

The Model 881 processor consists of a single Printed Circuit Board that normally occupies the first slot in the Series 5000 or 8000 Computer Systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus System.

The hardware on the 881 Processor Board consists of the following main functions.

- 8088 16-bit Microprocessor (CPU)
- 8087 Numeric Data Processor(Optional)
- 8259 Priority Vectored Interrupt Circuitry
- 58167 Real-Time Clock
- 2732 4K by 8 bit EPROM

SPECIFICATIONS

• Word Size:	Address	20 bits
	Data	16 bits
• On-Board ROM:		4Kbytes
• Directly Addressable Memory:		1Mbyte
• Clock Frequency:		4 MHz
• Circuit Board Dimensions:		5.25" x 10"

I/O DEVICE ADDRESSES FOR THE 881 CPU BOARD

06H-7FH	8259 Command and Status Select
60H-7FH	58167 Clock Internal Register Select
60H	R/W Counter - Thousandths of seconds
61H	R/W Counter - Hundredths and tenths of seconds
62H	R/W Counter - Seconds
63H	R/W Counter - Minutes
64H	R/W Counter - Hours
65H	R/W Counter - Day of the week
66H	R/W Counter - Day of the month
67H	R/W Counter - Months
68H	R/W Latches - Thousandths of seconds
69H	R/W Latches - Hundredths and tenths of seconds
6AH	R/W Latches - Seconds
6BH	R/W Latches - Minutes
6CH	R/W Latches - Hours
6DH	R/W Latches - Day of the week
6EH	R/W Latches - Day of the month
6FH	R/W Latches - Months
70H	R/O Interrupt Status Register
71H	W/O Interrupt Control Register
72H	W/O Counter Reset
73H	W/O Latch Reset
74H	R/O Status Bit
75H	W/O "GO" Command
76H	W/O Standby Interrupt
7FH	Test Mode

CONFIGURING THE 881 BOARD

EPROM Type Selection (JA)

If a 2716 (2K) EPROM is used in location 5B, then the upper pair of pins at location JA should be shunted. If the EPROM is a 2732 (4K) or a 2764 (8K), the lower pair should be shunted.

Numeric Processor Interrupt Enable (JB)

If the board has an 8087 in location 3B, location JB should be unshunted. If there is no 8087, JB should be shunted to mask out the numeric processor interrupt. Normally, JB is etched.

MWRT+ Enable (JC)

If this location is shunted, the MWRT+ signal (Memory Write) is sent out to the S-100 bus. Normally, it is unshunted.

Figure 2-9
Model 881 8088 Processor Board

2.5 MEMORY

2.5.1 MODEL 465 - 64K DYNAMIC RANDOM ACCESS MEMORY BOARD

The 465 board is the dynamic memory card. It contains 64K by 9 bits of memory space. The ninth bit in each byte is used as an odd parity check bit. The board can be used as separate 16K banks.

CONFIGURING THE 465 BOARD

465 boards shipped in IMS systems will normally be configured to the system requirements.

Phantom Line (Jack JD)

The phantom signal is activated when the system is "booting-up". When active, this line disables all memory except the Intial Program Loader EPROM. The phantom line affects memory read operations only, not memory write operations. When location JD is shunted, the phantom line is enabled. This location is etched for use in IMS systems. If this etch is cut, the phantom signal is ignored by the rest of the system.

Enable I/O (Jack JB)

When the memory is used in the bank mode or for parity operations, jack JB should be shunted so that the board can respond to I/O commands. Normally, JB is unshunted.

I/O Address Selection (Jack JC)

The selection of the board's I/O address is done on Jack JC. The jack is labeled 0-7 (top to bottom) for the respective address bits (A0-A7) of the I/O address. A "1" is programmed by removing a shunt. Therefore, to program I/O address 0FH, the top four shunts (0-3) would be removed ("1's") and the bottom four shunts (4-7) would be installed ("0's"). (Note that the "EN I/O" shunt must be on for the board to respond to the I/O command.) Normally, all positions are shunted.

CPU Selection (Jack JF)

The 8080 shunt (JF) should be installed for systems using 8080 CPUs. For Z-80 systems, this shunt should be removed.

Front Panel (Jack JH)

If the 465 board is to be used with an "IMSAI" front panel, the shunt JH must be in the right-most (FP) position. "IMSAI" front panels are mainly used for testing; in normal operation, this shunt should be in the leftmost position.

Memory Speed (Jack JA)

This shunt is dependent on the speed of the memory chips used, and it should always be in the L position.

Parity Error Interrupt Level (Jack JG)

Jack JG allows selection of eight different responses to a parity error. The selections are:

Shunt Position	Interrupt Selected
VI1	VECTORED INTERRUPT 1
VI2	VECTORED INTERRUPT 2
VI3	VECTORED INTERRUPT 3
VI4	VECTORED INTERRUPT 4
VI5	VECTORED INTERRUPT 5
INT	INT Line
NMI	Non-maskable INT (Z-80 Only)
RDY	PRDY Line (Parity Error Stops CPU)

The state of the parity circuit may be sensed by reading the I/O port on the memory board. If bit 0 is a "1", a parity error has occurred.

Normally, VI2 is shunted for CP/M systems; there are no shunts for TurboDOS.

Normal/Bank Mode (Jack JE)

This shunt should be installed only if the board is to be used in the Bank Switched mode. In the normal mode (unshunted) the board will respond to all addresses from 0000 to FFFF hex.

In the normal mode, with shunt JE removed, the four 16K memory banks occupy the entire 16 bit address space 0000 through FFFF hex. In this mode, each 16K bank may be controlled individually by an output to the board's I/O port. A "one" bit disables the associated bank. Control is on a bit basis, thus:

Output	Controlled Memory Bank (hex)
BIT 0=1	0000-3FFF
BIT 1=1	4000-7FFF
BIT 2=1	8000-BFFF (omitted in 32K vers.)
BIT 3=1	C000-FFFF (omitted in 32K & 48K vers.)

In the Bank Mode (Shunt JE installed) the board responds to a combination of bits. Codes are provided for a variety of configurations defined in the following table. Initially, the board is deselected by the Power On Clear signal. The 465 memory board can be used in a 16K, 32K or 48K bank selection scheme.

BANK MODE TABLE

Output Byte	Memory Mapping	
0	All Banks Deselected	
1	Banks 0 & 1 Occupy Addresses	8000-FFFF (32K)
2	Banks 2 & 3 Occupy Addresses	8000-FFFF (32K)
3	Banks 1, 2, & 3 Occupy Addresses	4000-FFFF (48K)
4	Bank 0 Occupies Addresses	4000-7FFF (16K)
5	Bank 0 Occupies Addresses	8000-BFFF (16K)
6	Bank 0 Occupies Addresses	C000-FFFF (16K)
7	Bank 1 Occupies Addresses	4000-7FFF (16K)
8	Bank 1 Occupies Addresses	8000-BFFF (16K)
9	Bank 1 Occupies Addresses	C000-FFFF (16K)
A	Bank 2 Occupies Addresses	4000-7FFF (16K)
B	Bank 2 Occupies Addresses	8000-BFFF (16K)
C	Bank 2 Occupies Addresses	C000-FFFF (16K)
D	Bank 3 Occupies Addresses	4000-7FFF (16K)
E	Bank 3 Occupies Addresses	8000-BFFF (16K)
F	Bank 3 Occupies Addresses	C000-FFFF (16K)

465 64KB DYNAMIC RAM BOARD STANDARD CONFIGURATION

Legend

Jack	Description	Standard Configuration
JA	Memory Speed	Normal position is L. On 464 Rev. A and previous revs, shunt is in the H position.
JB	En I/O	Open
JC	I/O Selection	All positions shunted
JD	Phantom Line	Shunted (etch)
JE	Normal/Bank Mode	Open
JF	CPU Selection	Open
JG	Parity Interrupt	All open for TurboDOS, VI2 shunted for CP/M & MP/M.
JH	Front Panel	Left position shunted.

NOTE. Four spare shunts are installed on the upper pins of Jack JG. These pins are all connected by etch and serve as a convenient place to store spare shunts.

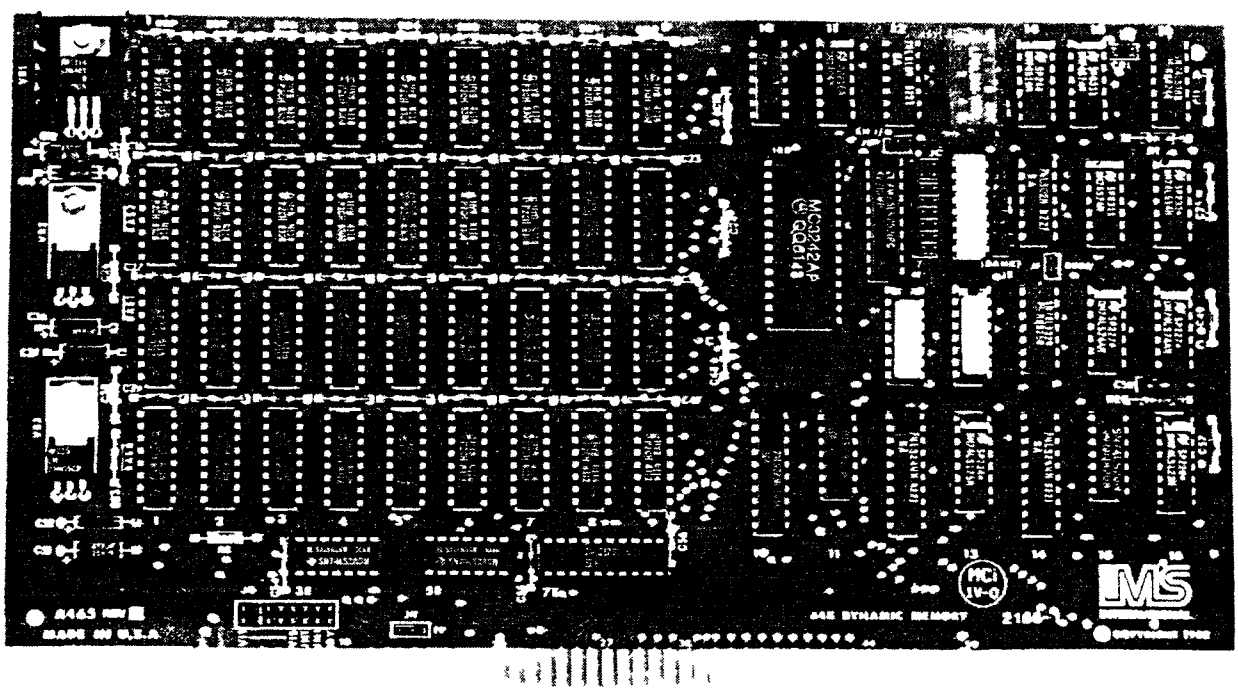


Figure 2-10
465 64KB Dynamic RAM Board

2.5.2 MODEL 961 - 256K DYNAMIC RAM BOARD

GENERAL DESCRIPTION

The Model 961 Memory Board uses 64K X 1 bit dynamic memory circuits. Boards are tested and burned in at an elevated temperature under diagnostic test to insure reliable operation.

A standard feature of the 961 board is byte parity checking which can generate an Interrupt or a Wait signal to the CPU if any single bit memory error occurs. A LED indicator on the board lights up to indicate an error. The CPU can then read the memory board's I/O port to clear the error indicator.

The Model 961 board has a "Phantom Signal" input for systems with ROM memories which use this feature. The phantom signal, when active, disables all memory except the Initial Program Loader ROM.

The 961 board decodes a full 20-bit address, allowing a system memory address capacity of 1 Megabyte. Switches allow the system to address the board as a 256K memory segment.

CONFIGURING THE 961 BOARD

Memory Board Address Select (JA)

Since there is a system memory capability of 1 megabyte, a 971 memory board can be used to supply a 256K segment of memory. Shunt JA is the segment select shunt, identifying which addresses the board will respond to.

JA-1	shunted	= addresses	00000-3FFFF
JA-2	shunted	= addresses	40000-7FFFF
JA-3	shunted	= addresses	80000-BFFFF
JA-4	shunted	= addresses	C0000-FFFFF

Parity Error Response Selection (JB)

Shunt JB selects the type of response the CPU will give to a parity error.

JB-1	shunted	= VI1 (Vectored Interrupt 1)
JB-2	shunted	= VI2 (Vectored Interrupt 2)
JB-3	shunted	= VI3 (Vectored Interrupt 3)
JB-4	shunted	= VI4 (Vectored Interrupt 4)
JB-5	shunted	= VI5 (Vectored Interrupt 5)
JB-6	shunted	= VI6 (Vectored Interrupt 6)
JB-7	shunted	= NMI (Non-Maskable Interrupt)
JB-8	shunted	= RDY (Hold CPU in a Wait condition)

The state of the parity circuit may be sensed by reading the I/O port on the memory board. If bit 0 contains a "1", a parity error has occurred.

The normal setting depends on the operating system used.

Phantom Signal (JC)

If a shunt is installed on JC, the board will be disabled by an activated Phantom Signal. The Phantom signal is used to disable all memory other than the Initial Program Loader while the system is starting up. In IMS systems, JC is unshunted.

I/O Device Address Select (JD)

The I/O Address for the memory board may be selected by shunts on JD. The shunts are labeled 1-8 for the respective address bits (A0-A7) of the I/O address. A "1" is programmed by removing a shunt. Normally, all the locations are shunted for a 00H I/O address.

JD-1 = A0
JD-2 = A1
JD-3 = A2
JD-4 = A3
JD-5 = A4
JD-6 = A5
JD-7 = A6
JD-8 = A7

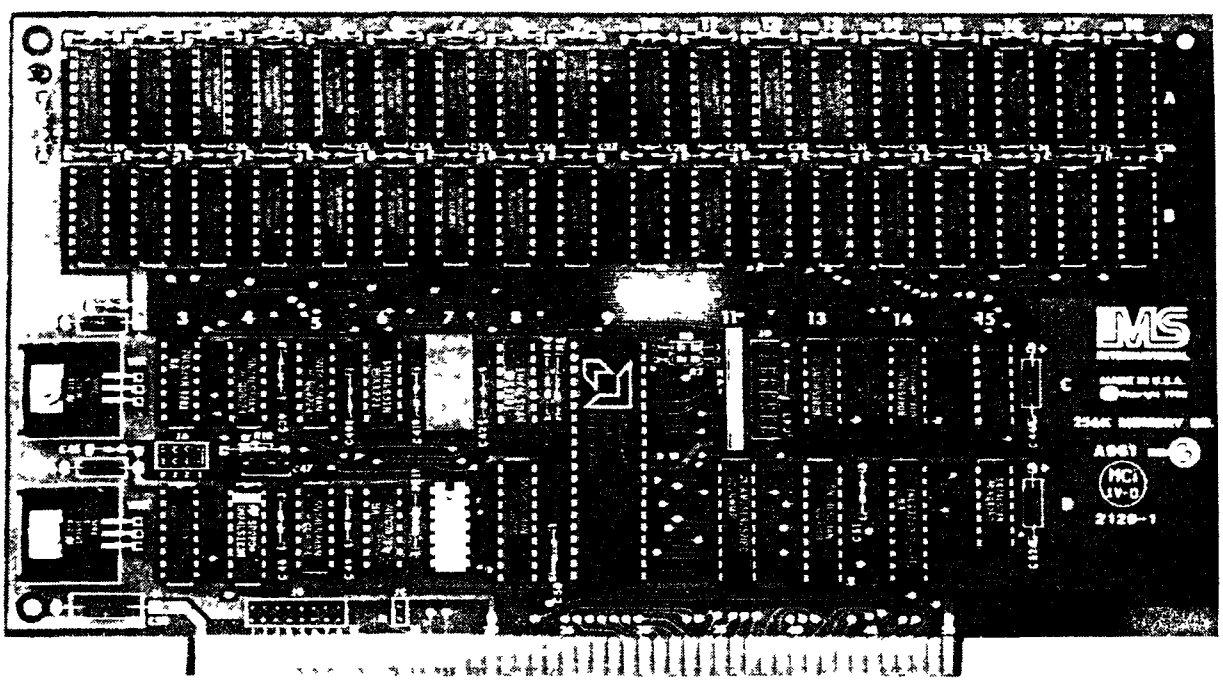


Figure 2-11 - Model 961 256K Memory Board

2.6 I/O CONTROLLERS

2.6.1 MODEL 444 I/O BOARD

FUNCTIONAL DESCRIPTION

The Model 444 I/O Board serves as an integral part of IMS 5000 and 8000 systems by providing timing and I/O interfacing for two serial and three 8-bit parallel ports.

Timing is provided by the Programmable Interval Timer (PIT). The PIT is a Timer/Counter and functions as a general-purpose timing element that generates relative time interrupts under software control.

The Universal Asynchronous Receiver/Transmitter (UART) interfaces the Z-80 microprocessor to an asynchronous serial data channel. The UART converts input serial data to parallel data to be used by the system. Output data is converted from parallel to serial and placed on the RS-232 port.

The Programmable Peripheral Interface circuit interfaces the Z-80 microprocessor to three 8-bit parallel ports. These parallel ports are located at the 50 pin I/O connector at the top of the 444 I/O board. Each line is TTL buffered and provides for termination. This parallel port can be programmed as input, output, or bidirectional I/O under software control.

FEATURES

- 2048 by 8-bit EPROM
- Programmable Interval Timer/Relative Time Clock
- Two UART's supplying baud rates from 75 to 19.2K baud.
- Two RS-232 ports with partial modem control
- Three 8-bit parallel ports

SPECIFICATIONS

. On-Board ROM:	Up to 4 Kbyte
. Serial I/O Ports:	2
. 8 Bit Parallel Ports:	3
. Baud Rates:	75 to 19.2K Baud
. Circuit board Dimensions:	5.25" x 10" (13.3 cm x 25.4 cm)
. Power Requirements:	+16V @ 60 ma +8V @ 500 ma -16V @ 40 ma

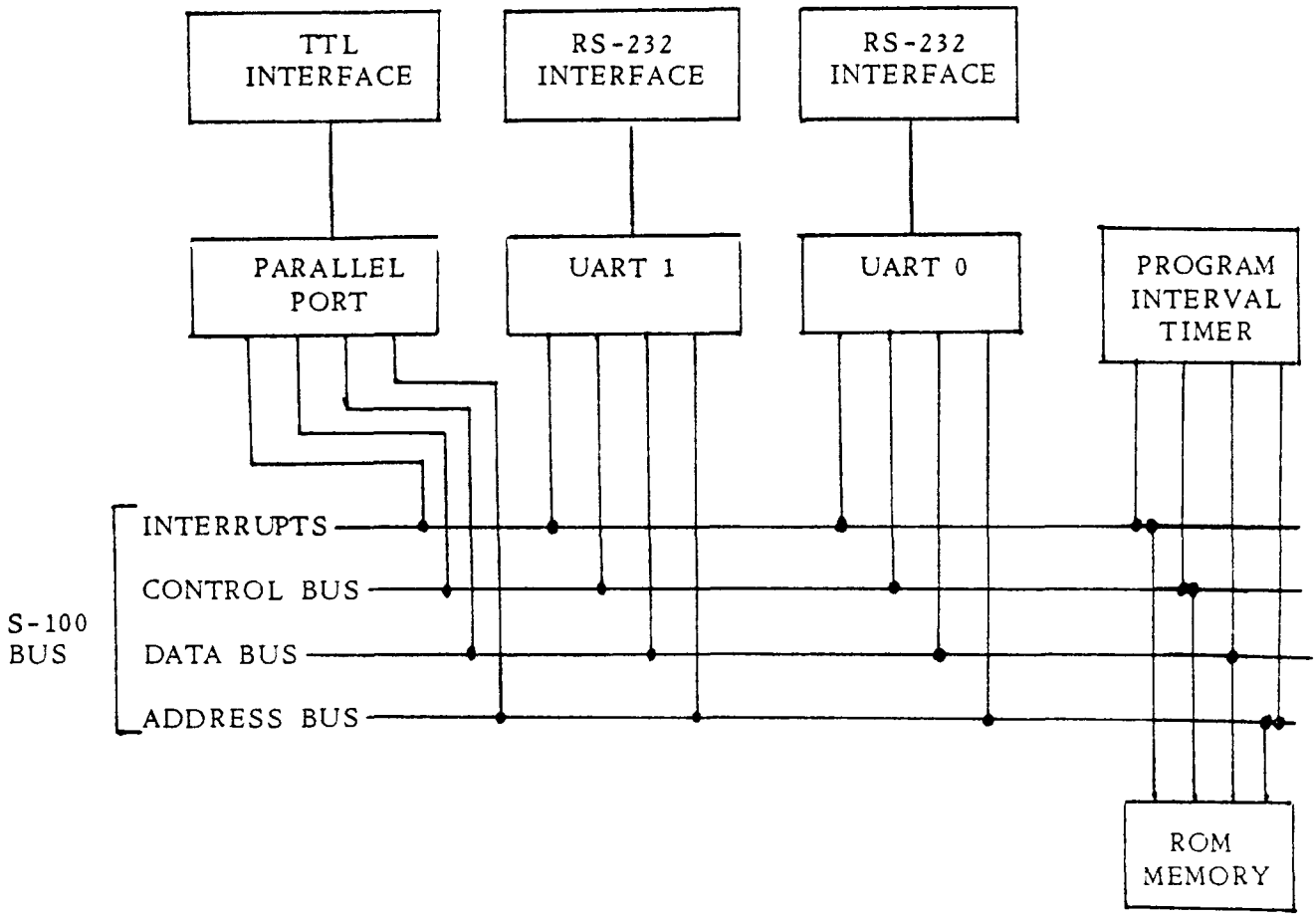


Figure 2-12
Model 444 Board Block Diagram

2048 x 8 EPROM

The 2716 EPROM contains the IMS Initial Program Loader (IPL). Its address space is shunt selectable.

Programmable Interval Timer (8253)

The 8253 functions as a general-purpose, multi-mode timing element that can be considered as an array of I/O ports.

The 8253 allows the programmer to set up timing loops in the system software to generate accurate time delays under software control. The user may initialize one of three counters with the desired quantity and, upon command, count out the delay and interrupt the CPU when it has completed its tasks. This minimizes software overhead and allows multiple delays that can be easily maintained by assignment of priority levels.

Other functions provided by the 8253 are:

- Relative Time Clock
- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Digital One-Shot

Universal Asynchronous Receiver/Transmitter (UART)

The 444 has two serial I/O ports. Each port consists of a UART and one-third of the programmable interval timer (PIT). The UART is a programmable device used for interfacing an asynchronous serial communication line to the parallel data lines of the microprocessor. It is made up of two separate and independent sections: the receiver and the transmitter.

The receiver accepts the serial data, decodes the control bits and converts the data bits to parallel data. The decode function converts the serial Start, Data, Parity, and Stop bits to parallel information and verifies the proper code transmission by checking parity and the receipt of a valid stop bit.

The transmitter section converts the parallel data into a serial word which contains the data, along with the start, parity, and stop bits.

Both the receiver and transmitter double-buffer data transfers with the processor. The UART may be programmed as follows:

1. The word length may be either 5, 6, 7, or 8 bits. (The IMS standard is 8 bits.)
2. Parity generation and checking may be inhibited, and the parity may be odd or even. (No parity standard for IMS systems.)
3. The number of stop bits may be one or two (1 1/2 when transmitting a 5-bit code).
   (IMS uses 1 stop bit.)
4. The baud rate may be set from 75 to 19.2K baud. (9600 baud is standard.)

I/O DEVICE ADDRESSES FOR THE 444 BOARD

X0H	Comm 0	Read/Write Control for UART 0
X1H	Comm 0	Read/Write Data for UART 0
X2H	Comm 1	Read/Write Control for UART 1
X3H	Comm 1	Read/Write Data for UART 1
X4H	Timer 0	Read/Write Data (Baud Clock * 16 Comm 0)
X5H	Timer 1	Read/Write Data (Baud Clock * 16 Comm 1)
X6H	Timer 2	Read/Write Data (RTC)
X7H	Timer Control Write	
X8H	Interrupt Enable - Request to Send Control	
X9H	Timer 2	Interrupt Reset (RTC)
XCH	Port A	Data
XDH	Port B	Data
XEH	Port C	Data
XFH	Parallel Control Write	

X=Base Address selected at location JP (If Address= 10H, then X=1. If Address= 20H, then X=2.) Usually, X=1.

SERIAL PORT CONNECTIONS

The two serial ports of the Model 444 I/O board communicate with peripherals using the RS-232 standard. The RS-232 interface standard is for the interconnection of data processing terminal equipment and data communication equipment. It defines a means of exchanging control signals and serial data between devices, and is of particular importance when each is furnished by a different company.

The 12 pin connector, J1, (top center of the 444 I/O board) connects the two UART's on the 444 board to the two DB25 female connectors mounted on the I/O panel at the rear of the IMS computer (CH. 1 and CH. 2). The internal cable connecting this 12 pin connector and the two female DB25 connectors is wired as follows:

444 Board (Connector J1)		**I/O Panel (CH.1 - Console Port)**
Pin #	Signal	Pin #
1	TX (Transmit Data)	2
2	RD (Receive Data)	3
4	CTS (Clear to Send)	5
3	RTS (Request to Send)	4
5	GND (Signal Ground)	7
		(CH.2 - Printer Port)
6	GND (Signal Ground)	7
8	RTS (Request to Send)	4
7	CTS (Clear to Send)	5
9	RD (Receive Data)	3
10	TX (Transmit Data)	2

Serial port 1 (CH. 1) is normally connected to the video terminal.

Serial port 2 (CH. 2) is normally connected to the serial printer.

To connect a CRT to the IMS system, you will need a cable with the following connections:

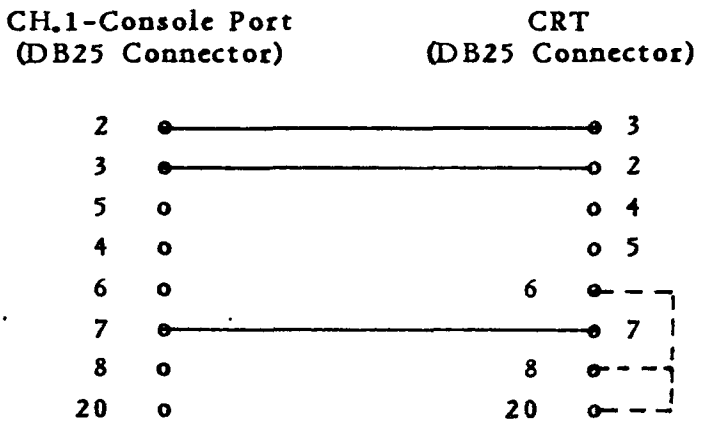


Figure 2-13 - Computer to CRT Connection (RS232)

Note: Refer to the CRT manual to determine if it is necessary to tie pins 4 and 5 and pins 6, 8, and 20 together. This requirement will vary from one CRT manufacturer to another.

To connect a printer to the IMS computer, you will need a cable with the connections shown below. This cable is used for CTS TI810/820, Okidata 82,83,84A, and Epson MX80 and MX100 printers.

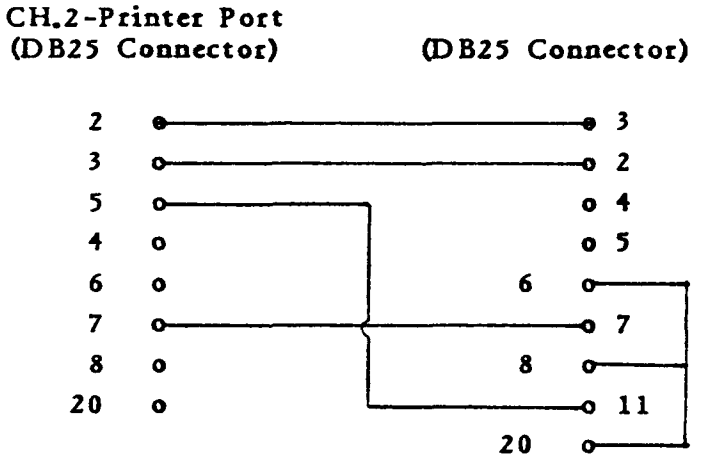


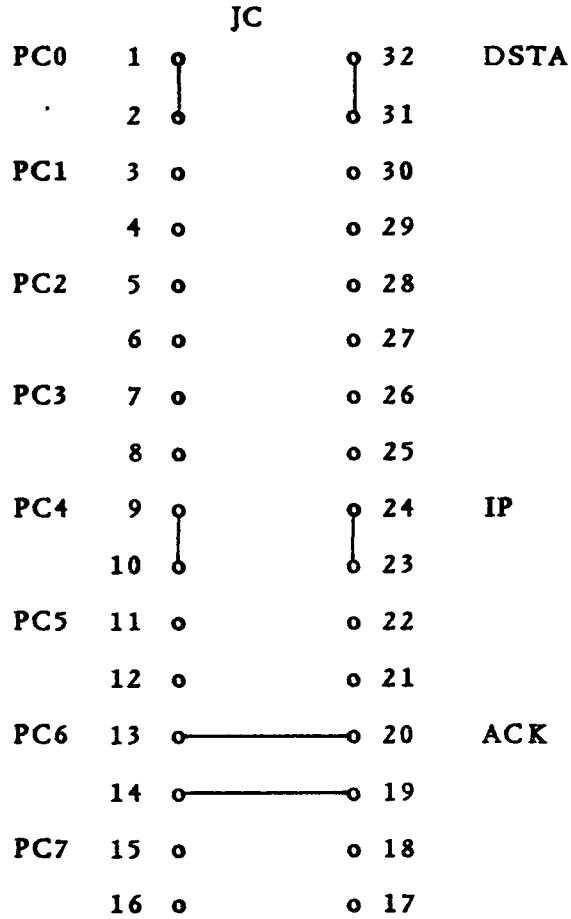
Figure 2-14 - Computer to Printer Connection (RS232)

USING A PARALLEL PRINTER

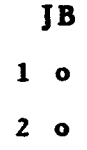
Using a Centronics Parallel Printer

To use a Centronics parallel printer, shunt locations JB and JC as shown below.

1. Shunt the following pins located at pad JC:



2. Remove shunt at pad JB.



A twisted pairs cable with the following connections is needed.

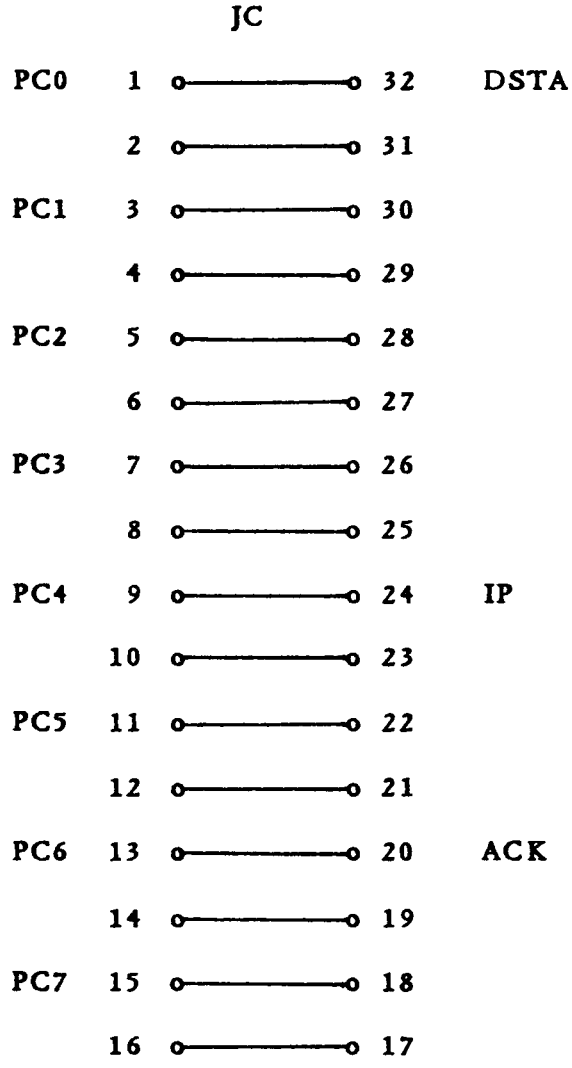
IMS COMPUTER 50 pin IDS Connector		CENTRONICS PRINTER Amphenol 57-30360 Connector	
PA7	3	9	DS8
GND	4	27	GND
PA6	5	8	DS7
GND	6	26	GND
PA5	7	7	DS6
GND	8	25	GND
PA4	9	6	DS5
GND	10	24	GND
PA3	11	5	DS4
GND	12	23	GND
PA2	13	4	DS3
GND	14	22	GND
PA1	15	3	DS2
GND	16	21	GND
PA0	17	2	DS1
GND	18	20	GND
PB3	27	11	BUSY
GND	28	29	GND
PB2	29	12	PE
PB1	31	13	SLCT
PB0	33	32	FAULT
GND	34	17	GND
PC6	37	10	ACK -
GND	38	28	GND
PC4	41	31	IP -
GND	42	30	GND
PC0	49	1	DSTA -
GND	50	19	GND

PAX = PARALLEL PORT A BITS
PBX = PARALLEL PORT B BITS
PCX = PARALLEL PORT C BITS

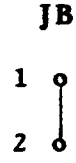
Figure 2-15
Computer to Centronics Printer Connection (14 Twisted Pairs Cable)

Using a NEC Spinwriter 5500D Parallel Printer

1. Install 16 horizontal shunts at pad JC (all pins shunted).



2. Install a vertical shunt at pad JB.



A cable with the following connections is needed.

PARALLEL NEC SPINWRITER PRINTER CABLE

IMS Computer 50 pin IDS Connector	NEC Spinwriter Printer 50 pin IDS Connector	Signal
3	45	Dataline 8
5	43	Dataline 7
7	42	Dataline 6
9	40	Dataline 5
11	33	Dataline 4
13	39	Dataline 3
15	36	Dataline 2
17	37	Dataline 1
19	10	Dataline 12
21	13	Restore
23	17	Carriage Strobe
25	15	Paper Feed Strobe
27	21	Print Wheel Strobe
29	9	Dataline 11
31	1	Dataline 10
33	46	Dataline 9
35	12	Check Status
37	3	Paper Out Status
39	4	Ribbon Out Status
41		(NOT USED)
43	27	Print Wheel Ready
45	34	Paper Feed Ready
47	26	Carriage Ready
49	28	Printer Ready

CONFIGURING THE 444 I/O BOARD

Parallel Port A Modes Selection (Location JA)

Shunt location JA indicates the direction of parallel port A.

JA	
1 o	o 4
2 o	o 3

No shunts = input mode
Shunt JA 1-4 = output mode
Shunt JA 2-3 = bi-directional mode

Parallel Port A Driver/Receiver Selection (Location 8A, 10A)

74LS243	non inverting
74LS242	inverting

Parallel Port A Termination Options (Location 9A)

Open = No termination
For Pull-Up, use a Beckman 899-1-R1.0K resistor pack.
For Pull-Up/Pull-Down, use a Beckman 899-5-R220/330 resistor pack.

Parallel Port B Mode Select (Location JB)

Shunt location JB indicates the mode of parallel port B.

JB	
1 o	Shunt JB 1-2 = output mode
2 o	

No shunt = input mode

Parallel Port B Driver/Receiver (Location 10B,11A)

74LS243	non inverting
74LS242	inverting

Parallel Port B Termination Options (Location 11B)

Open = No termination
For Pull-Up, use a Beckman 899-1-R1.0K resistor pack.
For Pull-Up/Pull-Down, use a Beckman 899-1-R220/330 resistor pack.

Parallel Port C Direction Select (Location JC)

The direction of each bit in Port C can be individually selected.

JC

1	**o**	**PC0**	**o**	**32**	
2	**o**		**o**	**31**	
3	**o**	**PC1**	**o**	**30**	
4	**o**		**o**	**29**	
5	**o**	**PC2**	**o**	**28**	No shunts = Bit unused
6	**o**		**o**	**27**	
7	**o**	**PC3**	**o**	**26**	Horizontal pair of shunts = input (receiver)
8	**o**		**o**	**25**	
9	**o**	**PC4**	**o**	**24**	Vertical pair of shunts = output (driver)
10	**o**		**o**	**23**	
11	**o**	**PC5**	**o**	**22**	
12	**o**		**o**	**21**	
13	**o**	**PC6**	**o**	**20**	
14	**o**		**o**	**19**	
15	**o**	**PC7**	**o**	**18**	
16	**o**		**o**	**17**	

Parallel Port C Driver/Receiver (Location 13A)

74LS244	non inverting
74LS240	inverting

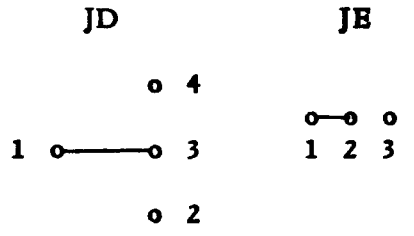
Parallel Port C Termination Options (Location 12A)

Open = no termination
For Pull-Up, insert a Beckman 899-1-R1.0K resistor pack.
For Pull-Up/Pull-Down, insert a Beckman 899-1-R220/330 resistor pack.

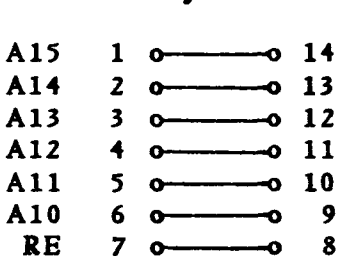
EPROM Selection (Locations JD,JE,JF,JG)

Any etched connections which are not defined in the following diagrams should be cut.

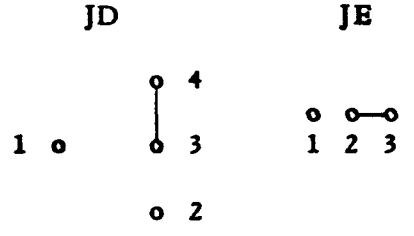
To Use a 2708 1K x 8 EPROM:



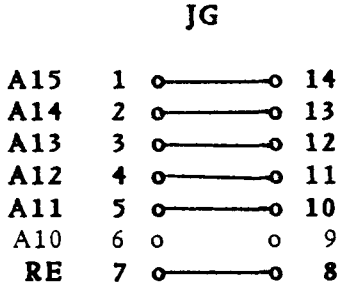
Shunt JD 1-3
Shunt JE 1-2
Shunt JF 1-2
Shunt JF 3-4
Shunt all horizontally at JG



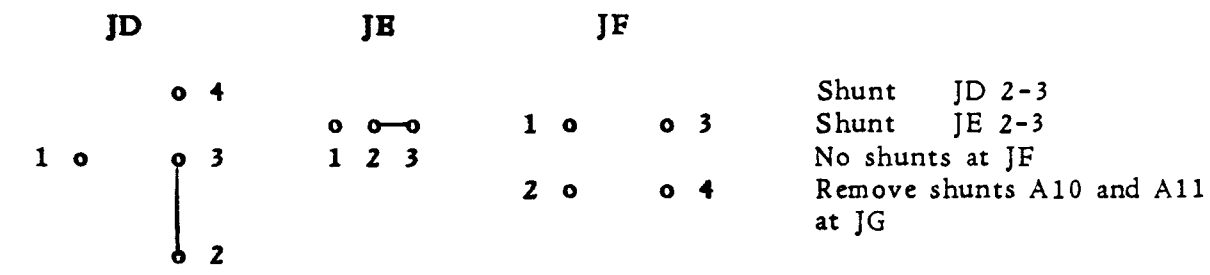
To Use a 2716 2K x 8 EPROM:

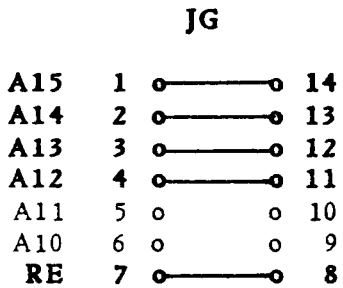


Shunt JD 3-4
Shunt JE 2-3
Shunt JF 3-4
Remove shunt A10 at JG

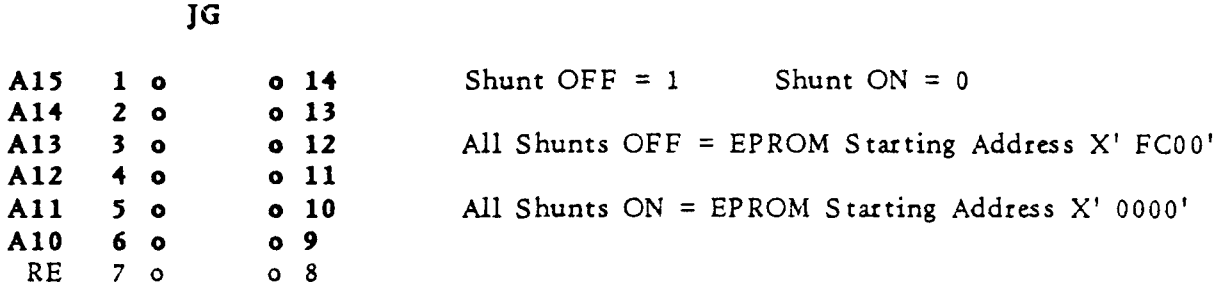


To Use a 2732 4K x 8 EPROM:

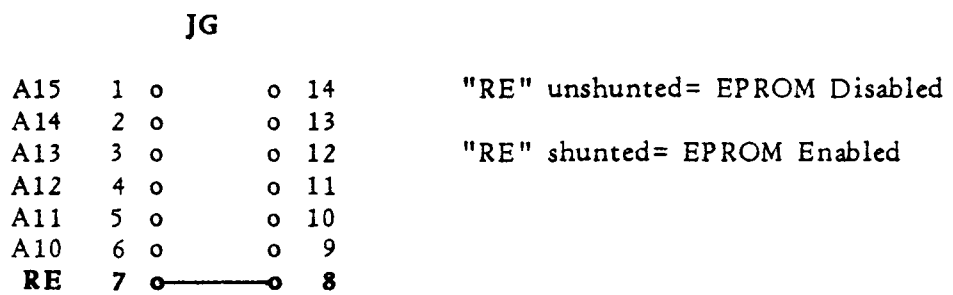




EPROM Address Selection (Location JG)



EPROM Enable (RE at Location JG)



Timer Clock Option (Location JH)

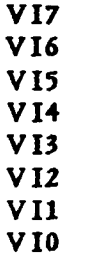
JH

Shunt JH 1-4 = Enable External 2Mhz Clock (75 to 9600 baud rate)
Shunt JH 2-3 = Enable on-board 1.2288 Mhz Clock (75 to 19200 baud rate)

Interrupt Options (Locations JJ, JK, JL, JM, JN)

The installation of a horizontal shunt will select the interrupt level for the functions listed below.

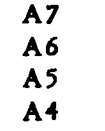
JJ - JN



JJ = Relative Time Clock (RTC) Interrupt
JK = Line 0 Transmit/Receive Interrupt
JL = Line 1 Transmit/Receive Interrupt
JM = Parallel Port B Interrupt
JN = Parallel Port A Interrupt

I/O Device Address Selection (Location JP)

JP



Shunt OFF = 1 Shunt ON = 0
All Shunts OFF = I/O Addresses F0H - FFH
All Shunts ON = I/O Addresses 00H - 0FH

Example:

Shunt A7, A6, A5 = I/O Address of 10 hex (Standard)
Shunt A7, A6, A4 = I/O Address of 20 hex
Shunt A7, A5, A4 = I/O Address of 40 hex

MODEL 444 BOARD STANDARD FACTORY CONFIGURATION

Legend

	Location and Description	Configuration
	Port Mode Selection	For Centronics Printer
1.	JA - Port A Mode Selection	Shunt 1-4
2.	JB - Port B Mode Selection	Shunt 1-2
3.	JC - Port C Selection	PC0 vertical shunts (output) PC4 vertical shunts (output) PC6 horizontal shunts (input)
	EPROM Selection	For 2716 EPROM
4.	JD - EPROM Selection	Shunt 3-4
5.	JE - EPROM Selection	Shunt 2-3
6.	JF - EPROM Selection	Shunt 3-4
7.	JG - EPROM Address Selection	Shunt all except A10. (Starting Address 0400H)
8.	JH - Optional Oscillator Enable	Shunt 2-3 (75 to 19200 baud)
9.	JJ - Relative Time Clock Interrupt	Shunt VI1
10.	JK - Line 0 Trans/Rec Interrupt	Shunt VI3
11.	JL - Line 1 Trans/Rec Interrupt	Shunt VI3
12.	JM - Port B Interrupt	No shunts
13.	JN - Port A Interrupt	No shunts
14.	JP - I/O Address Selection	Shunt all except A4 (Address 10H)

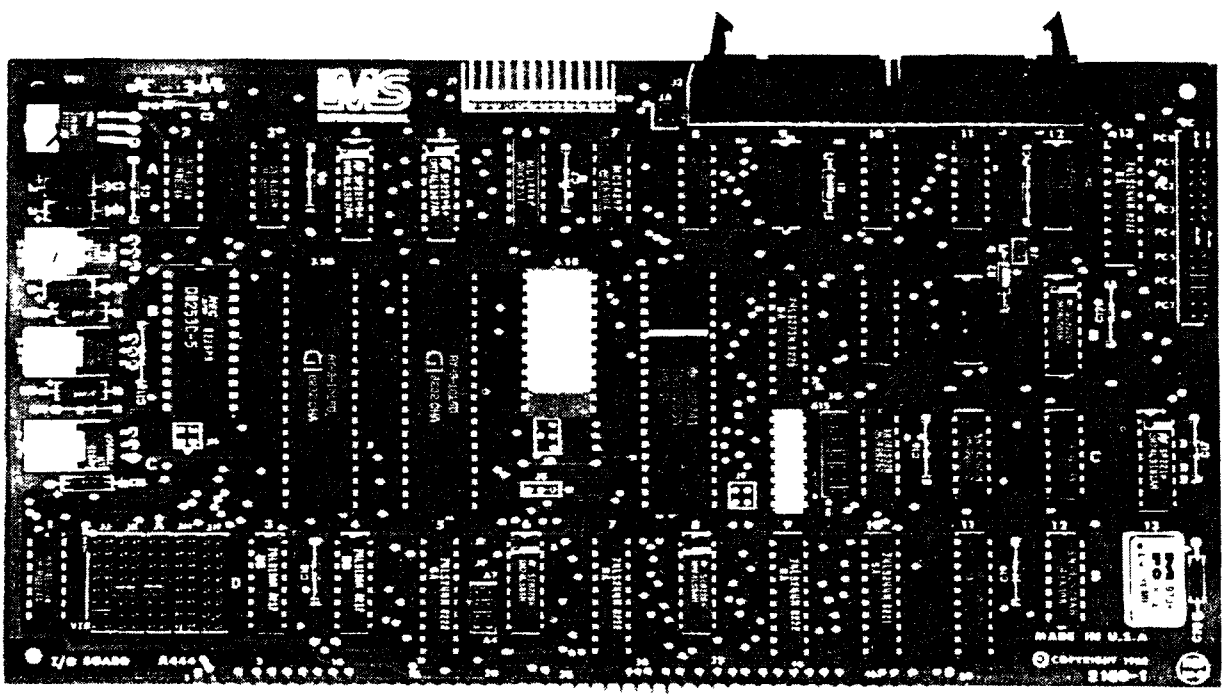


Figure 2-16 - Model 444 I/O Controller Board

2.6.2 MODEL 631 I/O CONTROLLER BOARD

GENERAL DESCRIPTION

The Model 631 I/O Controller has two asynchronous serial ports and three 8-bit parallel ports.

The 8250 Asynchronous Communication Element (ACE) converts input serial data from the RS-232C port to parallel data to be used by the system. Output data is converted from parallel to serial and placed on the RS-232C port.

The 8255 Programmable Peripheral Interface circuit interfaces the S-100 bus to three 8-bit parallel ports, which are located at J3, the 50 pin I/O connector at the top of the card. Each line is TTL buffered and provides for termination networks.

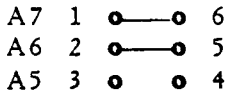
The Model 631 I/O Controller consists of a single printed circuit board which nominally occupies one slot in the Series 5000 or 8000 Computer Systems. Each serial RS-232C port is brought out to a 3M 26 pin header.

CONFIGURING THE 631 BOARD

I/O Address Selection (Location JA)

The most significant bits of the I/O addresses for the 631 board are selected at location JA. An address bit is a "1" if the shunt is removed, and a "0" if a shunt is installed. The correspondence of shunts to address bits is shown below. The normal address is 20H (A5 unshunted, A6 and A7 shunted).

JA

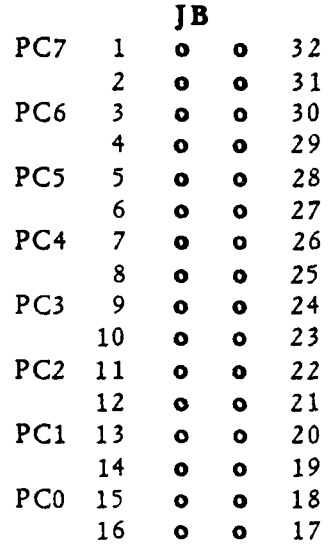


I/O Device Address Table

I/O Address(hex)	A7	A6	A5	SERIAL PORT 0	SERIAL PORT 1	PARALLEL PORTS
00-13	0	0	0	00-07	08-0F	10-13
20-33	0	0	1	20-27	28-2F	30-33
40-53	0	1	0	40-47	48-4F	50-53
60-73	0	1	1	60-67	68-6F	70-73
80-93	1	0	0	80-87	88-8F	90-93
A0-B3	1	0	1	A0-A7	A8-AF	B0-B3
C0-D3	1	1	0	C0-C7	C8-CF	D0-D3
E0-F3	1	1	1	E0-E7	E8-EF	F0-F3

Parallel Port C Bit Direction Selection (Location JB)

The direction of each bit in port C can be individually selected.



Bit unused -- no shunts.

Input -- pair of horizontal shunts

Output -- pair of vertical shunts

Port C Driver/Receiver Selection (Location 11C)

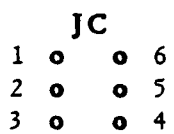
74LS240 = Inverting
74LS244 = Non Inverting

Port C Termination Options (Location 9A)

Open	= No Termination
1K Pull Up	= Beckman 899-1-R1.0K
220/330 Pull Up/Pull Down	= Beckman 899-5-R220/330

Parallel Port A Mode Selection (Location JC)

Shunt location JC indicates the direction of parallel port A.



NO SHUNTS = Output mode
SHUNT JC 1-6 = Bidirectional mode controlled by PC7
SHUNT JC 2-5 = Bidirectional mode controlled by PC6
SHUNT JC 3-4 = Input mode

Port A Driver/Receiver Selection (Location 9B)

8303 = Inverting
8304 = Non-Inverting

Port A Termination Options (LOC. 10A)

```
Open                          = No Termination
1K Pull Up                    = Beckman 899-1-R1.0K
220/330 Pull Up/Pull Down     = Beckman 899-5-R220/330
```

Parallel Port B Mode Selection (Location JD)

```
     JD
1  o                NO SHUNT       = Output Mode
2  o                SHUNT JD 1-2   = Input Mode
```

Port B Driver/Receiver Selection (Location 7C)

```
8303 = Inverting
8304 = Non-Inverting
```

Port B Termination Options (Location 8A)

```
Open                          = No Termination
1K Pull UP                    = Beckman 899-1-R1.0K
220/330 Pull Up/Pull Down     = Beckman 899-5-R220/330
```

Interrupt Level Selection (Locations JF,JG,JH,JJ)

```
        JF-JJ

VI7  1  o   o  16
VI6  2  o   o  15
VI5  3  o   o  14
VI4  4  o   o  13
VI3  5  o   o  12
VI2  6  o   o  11
VI1  7  o   o  10
VI0  8  o   o   9
```

Installing a shunt will select the Interrupt level for the ports listed below.

```
JF = Serial Port 0 Interrupt
JG = Serial Port 1 Interrupt
JH = Parallel Port B Interrupt (PC0 INTRB)
JJ = Parallel Port A Interrupt (PC3 INTRA)
```

SERIAL PORT CONNECTIONS

The two connectors, J1 and J2, on the upper edge of the board are connected to the I/O panel on the rear of the computer. If the system has a 645 processor board, J1 and J2 are connected to channels 1 and 2 respectively. Usually Channel 1 is connected to a terminal, and Channel 2 is connected to a serial printer. If the 631 board is used to increase I/O capability in a more recent version J1 and J2 are connected the next pair of free channels after the slave channels. The internal cables have the following connections:

Signal Name	RS-232 Circuit	631 Board J(x) pin #	I/O Panel DTE Connector (DB25) pin #
Transmit Data	BA	3	2
Receive Data	BB	5	3
Request to Send	CA	7	4
Clear to Send	CB	9	5
Data Set Ready	CC	11	6
Signal Ground	AB	13	7
Data Terminal Ready	CD	14	20
Data Carrier Detect	CF	15	8
Ring Indicator	CE	18	2

Figure 2-17 631 Board to I/O Panel Connection (RS-232)

Channel 1 is connected to a CRT using a cable with the following connections:

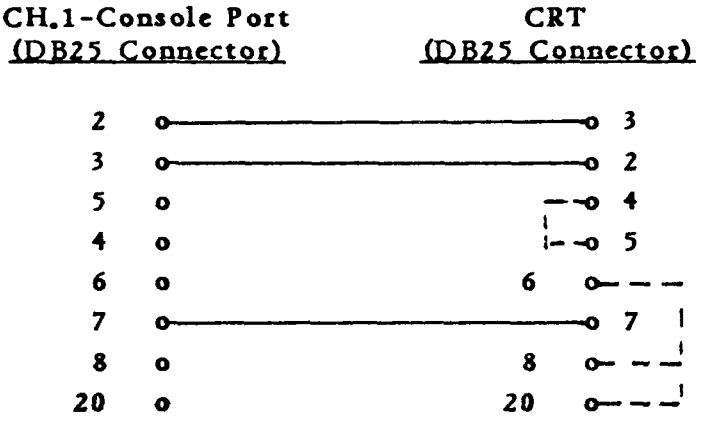


Figure 2-18 Computer to CRT Connection (RS-232)

Note: Refer to the CRT manual to determine if it is necessary to tie pins 4 and 5 and pins 6, 8, and 20 together. This requirement will vary from one CRT manufacturer to another.

Channel 2 is connected to a serial printer using the cable connections shown below. This cable is used for CTS TI810/820, Okidata 82,83,84A and Epson MX80 and MX100 serial printers.

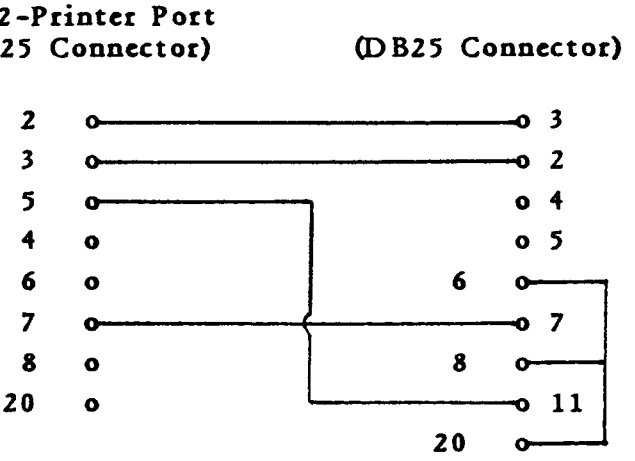


Figure 2-19 Computer to Serial Printer Connection (RS-232)

PARALLEL PORT CONNECTIONS

Connector J3 on the upper edge of the 631 is connected to the parallel data port on the I/O panel using a flat ribbon cable. The signals are listed below.

1. PB1	2. GND	27. PC3	28. PC0
3. PC6	4. PC5	29. GND	30.
5. PC4	6. GND	31.	32. GND
7.	8. GND	33. PA3	34. PC2
9. PB2	10. PB7	35. GND	36. PA1
11. GND	12. PC7	37. PA0	38. GND
13. PB6	14. GND	39. PA2	40. PA4
15. PB4	16. GND	41. GND	42. PA5
17. PB5	18. GND	43. PA6	44. GND
19.	20. GND	45. PA7	46. PB0
21. PB3	22. GND	47. GND	48.
23. GND	24. GND	49.	50. GND
25. GND	26. PC1		

PAx - Parallel Port A bits
PBx - Parallel Port B bits
PCx - Parallel Port C bits

Figure 2-20 631 Parallel Port Pin Listing

Using a NEC Parallel Printer

This cable connects the NEC Printer to the I/O panel, and is made from a 50 conductor ribbon cable with a 3M socket connector.

I/O Signal	Pin	NEC Signal
PA7	45	Dataline 8
PA6	43	Dataline 7
PA5	42	Dataline 6
PA4	40	Dataline 5
PA3	33	Dataline 4
PA2	39	Dataline 3
PA1	36	Dataline 2
PA0	37	Dataline 1
PB7	10	Dataline 12
PB6	13	Restore
PB5	17	Carriage Strobe
PB4	15	Paper Feed Strobe
PB3	21	Print Wheel Strobe
PB2	9	Dataline 11
PB1	1	Dataline 10
PB0	46	Dataline 9
PC7	12	Check Status
PC6	3	Paper Out Status
PC5	4	Ribbon Out Status
PC4	5	Cover Open
PC3	27	Print Wheel Ready
PC2	34	Paper Feed Ready
PC1	26	Carriage Ready
PC0	28	Printer Ready
GND	24	Select Printer
GND	23	Ribbon Lift

Note: Ground is on pins: 2,6,8,11,14,16,18,20,22,25,29,32,35,38,41,44,47,50

Figure 2-21 Computer to NEC Printer Connection

The following shunt connections need to be made for use of a NEC printer.

Location JB - all horizontal shunts (Port C - output)
Location JC - no shunt (Port A - output)
Location JD - no shunt (Port B - output)

Using a Centronics Parallel Printer

A cable with the connections shown below is used for connecting a Centronics parallel printer to the I/O panel data channel.

I/O Signal	Pin	Pin	Centronics Signal
PA7	45	9	DS8
PA6	43	8	DS7
PA5	42	7	DS6
PA4	40	6	DS5
PA3	33	5	DS4
PA2	39	4	DS3
PA1	36	3	DS2
PA0	37	2	DS1
PB3	21	11	Busy
PB2	9	12	PE
PB1	1	13	SLCT
PB0	46	32	Fault
PC6	3	10	ACK-
PC4	5	31	IP-
PC0	28	1	DSTA-

I/O Board Grounds 50,44,41,24,32,23,35,38,22,47, 2, 6,29
Centronics Grounds 27,26,25,24,23,22,21,20,29,17,28,30,19

Figure 2-22 Computer to Centronics Printer Connection

The following locations need to be shunted for use with the Centronics printer.

Location JB 3-30
4-29 (PC6 input)

15-16
17-18 (PC0 output)

7-8
25-26 (PC4 output)

Location JC No shunts.

Location JD 1-2

MODEL 631 I/O BOARD

Legend

Location	
JA	I/O Address Select Normally 20H. (A5 unshunted, A6 and A7 shunted).
JB	Parallel Port C Select Normal Shunting: (for Centronics printer) PC6 - Horizontal pair PC4 - Vertical pair PC0 - Vertical pair
JC	Parallel Port A Direction Select Normal = no shunt (for Centronics printer)
JD	Parallel Port B Direction Select Normal = shunted (for Centronics printer)
JF	Serial channel 0 Transmit/Receive Interrupt Normally VI3.
JG	Serial Channel 1 Transmit/Receive Interrupt Normally VI3.
JH	Parallel Port B Interrupt Normally unshunted.
JJ	Parallel Port A Interrupt Normally unshunted.
J1	Serial Port 0 (usually connected to channel 1)
J2	Serial Port 1 (usually connected to channel 2)
J3	Parallel Port (connected to parallel printer port)

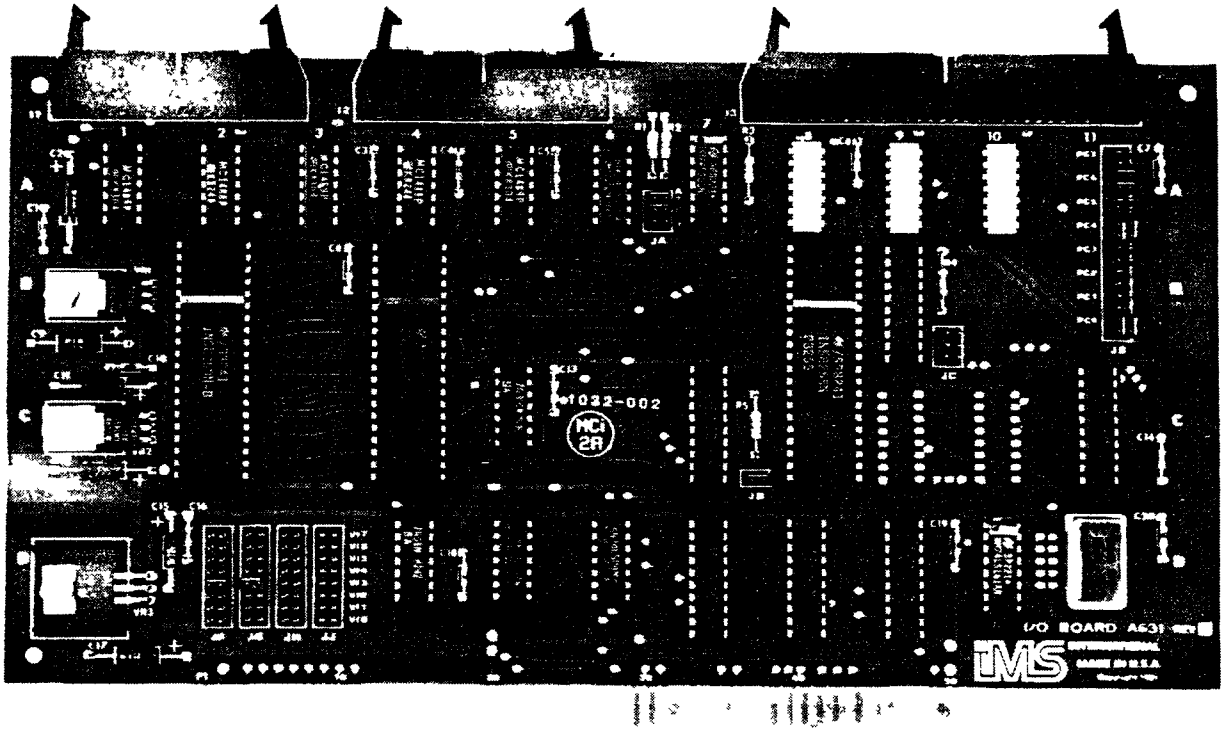


Figure 2-23
Model 631 I/O Controller Board

2.6.3 MODEL 480
FOUR-LINE ASYNCHRONOUS COMMUNICATIONS CONTROLLER

The IMS Model 480 has four RS-232 serial ports, controlled by the 8250 Asynchronous Communication Element (ACE).

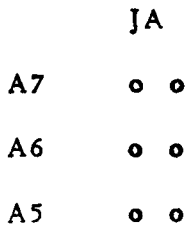
The Model 480 controller requires one slot in the S-100 bus. Each serial port is brought to a 3M 26 pin header on the I/O panel on the back of the machine.

CONFIGURING THE 480 BOARD

I/O Address Select (JA)

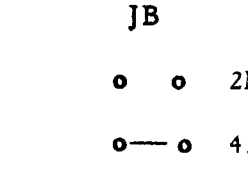
The most significant bits of the I/O addresses used by the 480 board are selected at location JA. Each shunt indicates the value for one address bit. The relation of shunts to address bits is shown below. If a shunt is removed, the corresponding address bit has a value of "1"; if a shunt is installed, the bit has a "0" value. So at location JA, if bits A7, A6 and A5 are unshunted, the 480 board addresses are E0H to FFH. With all the shunts on, the addresses are in the range 00H to 1FH.

Normally, A7 and A6 are shunted and A5 is unshunted, resulting in an I/O address of 20H. If the 4SIO (480) board is used as an additional I/O board, the address is E0H (all unshunted).



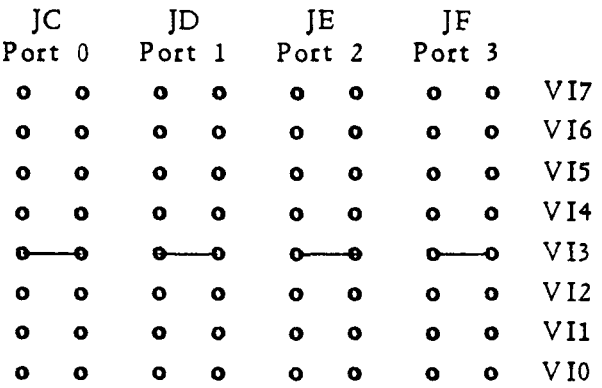
Baud Clock Option (JB)

With the lower pair shunted, baud rates to 19.2 Kbaud are allowed. With the upper pair shunted, the board uses the 2MHz base and allows up to 7600 baud to be generated. In normal operation, the lower pair is shunted.



Interrupt Level Selection (locations JC, JD, JE, JF)

Locations JC, JD, JE and JF allow the user to select the interrupt level for each port. In a standard system, VI3 is shunted for all four ports.



PORT CONNECTIONS

The four serial ports are connected to four connectors on the I/O panel using cables with the following connections:

Signal Name	RS-232C Circuit	480 Board J(X) Pin Number	I/O Panel Connector Pin Number
Transmit Data (Data to Modem)	BA	3	2
Receive Data (Data from Modem)	BB	5	3
Request to Send	CA	7	4
Clear to Send	CB	9	5
Data Set Ready	CC	11	6
Signal Ground	AB	13	7
Data Terminal Ready	CD	14	20
Data Carrier Detect	CF	15	8
Ring Indicator	CE	18	22

MODEL 480 BOARD STANDARD FACTORY CONFIGURATION

Legend

Jack

JA	I/O Address Select Normally 20H in "C" version of system. A7 = shunt A6 = shunt A5 = no shunt
JB	Oscillator Option: Normally lower pair is shunted.
JC	VI3 - shunted
JD	VI3 - shunted
JE	VI3 - shunted
JF	VI3 - shunted

Serial port 0 - Pin 1 on left
Serial port 1 - Pin 1 on left
Serial port 2 - Pin 1 on left
Serial port 3 - Pin 1 on left

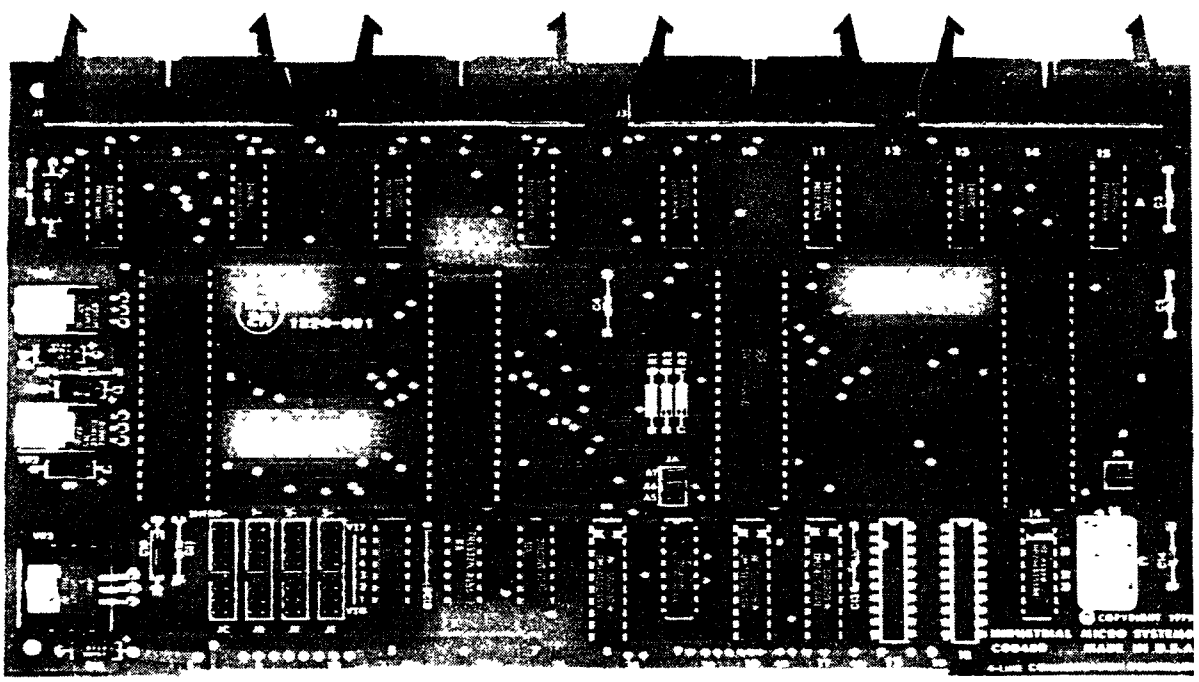


Figure 2-24 Model 480 I/O Controller Board

2.7 MULTIPROCESSOR BOARDS

2.7.1 MODEL 740 I/O PROCESSOR BOARD

GENERAL DESCRIPTION

The Model 740 board is used to add multi-user capability to an IMS system. It contains a processor, memory, and serial and parallel I/O ports. One 740 board is used for each additional user.

The 740 I/O Processor board consists of a single printed circuit board that occupies one slot in the Series 5000 or 8000 Computer Systems. Each serial RS-232C port is brought out to a 3M 26-pin header on the I/O panel.

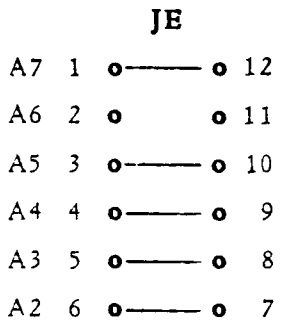
SPECIFICATIONS

Processor:	4MHz Z-80A CPU
Instruction set:	158 instructions
PROM Capacity:	2K bytes
PROM Type:	2716 or equivalent
RAM Capacity:	64K bytes with Parity
RAM Type:	4164 Dynamic
Serial Channels:	Two Asynchronous or Synchronous channels with modem control
Serial Channel Type:	Z-80A SIO/0 (or Z-80A DART Asynchronous Only)
Parallel Channel:	Ten bit-programmable parallel I/O lines compatible with Bell 801 Automatic Calling Unit
Parallel Channel Type:	Z-80A PIO
Parallel Channel:	24 bit programmable parallel I/O lines compatible with the S-100 bus for Host interface
Parallel Channel Type:	8255A PPI
Interval Timers:	4 Timers; two for baud rate control and two cascaded for programmable time interval
Timer Type:	Z-80A CTC
Vectored Interrupts:	Internally prioritized vector interrupt structure of the Z-80A microprocessor
Power Requirements:	+ 8 volts @ 800 ma +16 volts @ 80 ma -16 volts @ 70 ma
Operating Environment:	0-55 deg C

CONFIGURING THE MODEL 740 MPU

I/O Address Selection (Location JE)

The most significant bits of the I/O addresses used by the 740 board are defined at location JE. The correspondence between shunts and address bits are shown below. If a shunt is installed, the address bits are shown below. If a shunt is installed, the address bit has a '0' value; if the shunt is removed, the address bit has a value of '1'. The example below results in I/O addresses of 40H to 43H.



A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	X	X

Address Byte - 40H shown

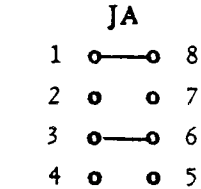
Example shown places 740 board at I/O addresses 40H - 43H.

When a system has more than one 740 board, each must have a different address, as shown below:

Board	I/O Address	Board	I/O Address
1st	40H	9th	E0H
2nd	44H	10th	E4H
3rd	48H	11th	E8H
4th	4CH	12th	ECH
5th	50H	13th	F0H
6th	54H	14th	F4H
7th	58H	15th	F8H
8th	5CH	16th	FGH

Port A Receive and Transmit Baud Clock Selection (JA)

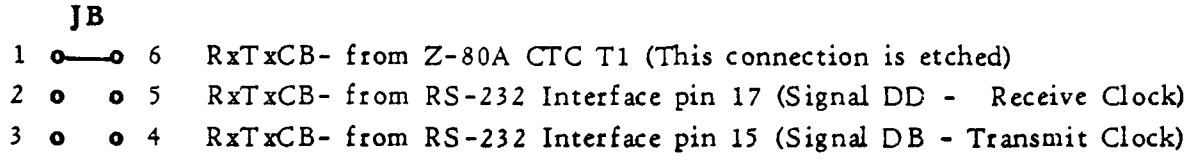
The upper two pairs of pins at location JA allow the user to choose the source of the "Receive" clock for port A. The lower two pairs select the source of the transmit clock signal. Normally, they are shunted as shown below.



RxCA- from Z-80A CTC T0 (This connection is etched.)
RxCA- from RS-232 Interface pin 17 (Signal DD - Receive Clock)
TxCA- from Z-80A CTC T0 (This connection requires a shunt.)
TxCA- from RS-232 Interface pin 15 (Signal DB - Transmit Clock)

Port B Receive and Transmit Baud Clock Selections (JB)

Location JB defines the source of port B's receive and transmit clocks. The normal connect is etched and shown below.



S-100 Reset Disable (Location JD)

A shunt in this location disables the RESET signal going to the 8255 chip. This location is only shunted during testing; normally it is unshunted.

SERIAL PORT CONNECTIONS

The two leftmost connectors on the upper edge of the board, J1 and J2, are connected to the I/O panel using a cable with the following connections.

Signal Name	RS-232C Circuit	740 Board J1 or J2 Connector Pin Number	I/O Panel Channel Pin Number
Protective ground	AA	1	1
Signal Ground	AB	13	7
Transmit Data	BA	3	2
Receive Data	BB	5	3
Request to Send	CA	7	4
Clear to Send	CB	9	5
Data Set Ready	CC	11	6
Data Terminal Ready	CD	14	20
Ring Indicator	CE	18	22
Data Carrier Detect	CF	15	8
Transmit Clock	DB	4	15
Receive Clock	DD	8	17

J1 and J2 on the first 740 board are usually connected to channels 3 and 4, respectively. The next 740 is usually connected to channels 5 and 6, the third 740 to channels 7 and 8, etc.

PARALLEL PORT CONNECTIONS

Connector J3 on the right side of the upper edge of the board is a 10 bit parallel port compatible with the Bell 801 Automatic Calling Unit. It is connected to the I/O panel by using a cable with the following connections:

Signal Name	ACU Circuit	740 Board J3 Connector Pin Number	I/O Panel Channel Pin Number
Frame ground	FGD	1	1
Signal Ground	SGD	13	7
Digit Present	DPR	3	2
Abandon Call-Retry	ACR	5	3
Call Request	CRQ	7	4
Present Next Digit	PND	9	5
Power Indication	PWI	11	6
Data Set Status	DSS	25	13
Number Bit 1	NB1	2	14
Number Bit 2	NB2	4	15
Number Bit 4	NB4	6	16
Number Bit 8	NB8	8	17
Data Line Occupied	DLO	18	22

MODEL 740 MULTIPROCESSOR BOARD

Legend

Jack	
JA	Received and Transmit Baud Clock Selection Normally 1-8 and 3-6 are shunted
JB	Receive and Transmit Baud Clock Selections Normally 1-6 is etched
JD	Reset Disable Shunt Normally unshunted
JE	I/O Device Address Selection
JF	Interrupt level for the 8255. Normally unshunted.
J1, J2	RS-232C Parallel Port Connectors
J3	Bell 801 Parallel Port Connector

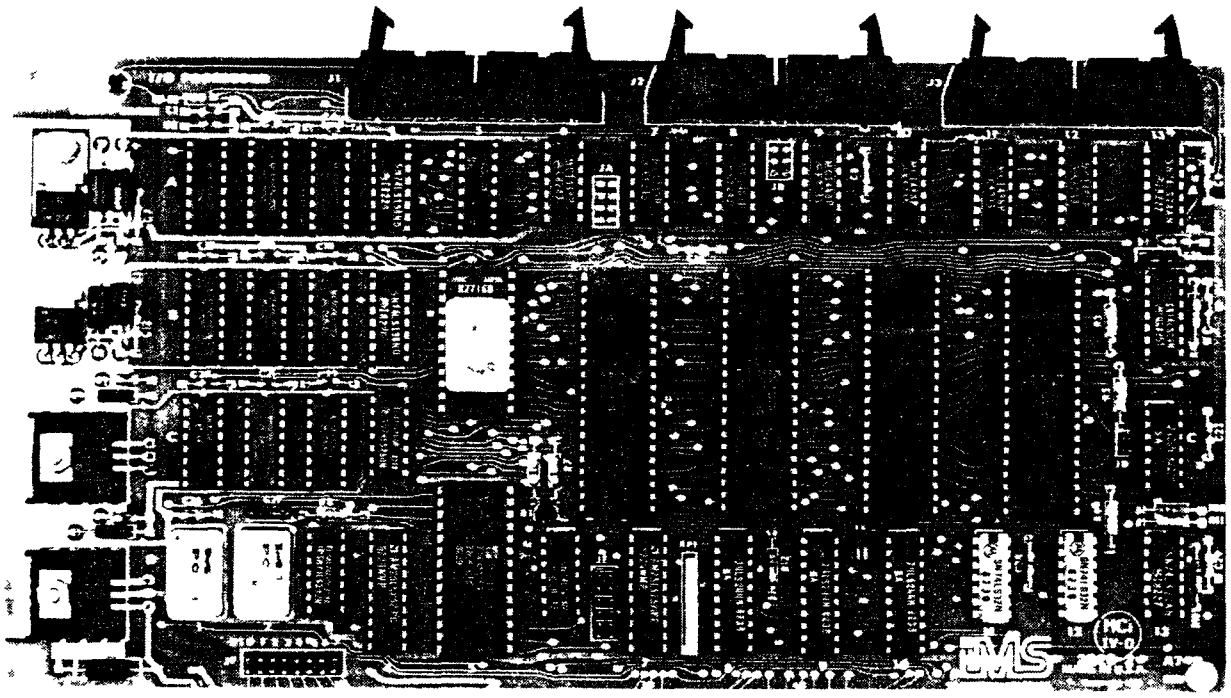


Figure 2-25 Model 740 Multiprocessor Board

2.7.2 MODEL 861 MULTIPROCESSOR UNIT

GENERAL DESCRIPTION

The Model 861 MPU is a single board computer with a processor, memory, and two serial I/O ports. It is used to add multi-user capability to the system.

The Model 861 MPU consists of a single printed circuit board that occupies one slot in the Series 5000 or 8000 Computer Systems. Each serial RS-232C port is brought out to a 3M 26-pin header on the I/O panel.

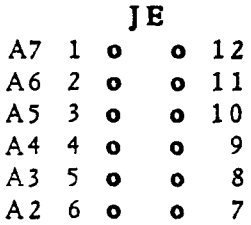
SPECIFICATIONS

Processor:	4MHz Z-80A CPU
Instruction set:	158 instructions
PROM Capacity:	2K bytes
PROM Type:	2716 or equivalent
RAM Capacity:	64K bytes with Parity
RAM Type:	4164 Dynamic
Serial Channels:	Two asynchronous or synchronous channels with modem control
Serial Channel Type:	Z-80A SIO/0 (or Z-80A DART asynchronous only)
Parallel Channel:	24 bit programmable parallel I/O lines compatible with the S-100 bus for host interface
Parallel Channel Type:	8255A PPI
Interval Timers:	4 timers; two for baud rate control and two cascaded for programmable time interval
Timer Type:	Z-80A CTC
Vectored Interrupts:	Internally prioritized vector interrupt structure of the Z-80A microprocessor
Power Requirements:	+ 8 volts @ 800ma +16 volts @ 80ma -16 volts @ 70ma
Operating Environment:	0-55 deg C

CONFIGURING THE 861 BOARD

I/O Address Selection (Location JE)

The most significant bits of the I/O addresses used by the 861 board are assigned values according to the shunts at location JE. If a shunt is on, the corresponding address bit has a '0' value; if a shunt is off, the bit has a '1' value.

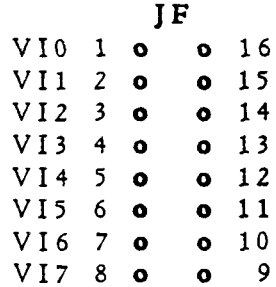


Each 861 board is assigned a unique address according to the table below:

Board	I/O Address		Board	I/O Address	
	Hex	Binary		Hex	Binary
1st	40H	010000XX	9th	E0H	111000XX
2nd	44H	010001XX	10th	E4H	111001XX
3rd	48H	010010XX	11th	E8H	111010XX
4th	4CH	010011XX	12th	ECH	111011XX
5th	50H	010100XX	13th	F0H	111100XX
6th	54H	010101XX	14th	F4H	111101XX
7th	58H	010110XX	15th	F8H	111110XX
8th	5CH	010111XX	16th	FCH	111111XX

Interrupt Level Selection (Location JF)

The interrupt level for the 861 board can be selected by a shunt on JF.



Port A Receive and Transmit Baud Clock Selection (JA)

The shunts at location JA indicate the source of the Receive and Transmit clocks for the serial ports. Normally, pins 1 and 16 are shunted, pins 3 and 14 are shunted, and pins 6 and 11 are shunted together.

```
   JA
 1o   o16  RxDA from RS-232 (Signal BB - Receive Data)
 2o   o15  RxDA from RS-422 (Signal RD - Receive Data)
 3o   o14  RxCA- from Z-80A CTC T0
 4o   o13  RxCA- from RS-232 (Signal DD - Receive Clock)
 5o   o12  RxCA- from RS-422 (Signal RT - Receive Timing)
 6o   o11  TxCA- from Z-80A CTC T0
 7o   o10  TxCA- from RS-232 (Signal DB - Transmit Clock)
 8o   o 9  TxCA- from Z-80A CTC T0/2
```

Port B Receive Clock Selections (JB)

The shunt at JB indicates the source of the 'receive' clock for port B. Normally, pins 1 and 4 are shunted.

```
   JB
 1o   o4  RxDB from RS-232 (Signal BB - Receive Data)
 2o   o3  RxDB from RS-422 (Signal RD - Receive Data)
```

Reset Disable (Location JD)

A shunt at location JD disables the RESET signal to the 861 board. JD is only shunted during testing; normally there is no shunt.

```
   JD
 1o       Normal mode - shunt off.
 2o       Local 861 test mode - shunt on.
```

PORT CONNECTIONS

The 861 is connected to the I/O panel using a flat ribbon cable. The pins and signals are given below:

Signal Name	RS-232C Circuit	Pin	
Signal Ground	AB	7	
Transmit Data	BA	2	(Data to MODEM)
Receive Data	BB	3	(Data from MODEM)
Request To Send	CA	4	
Clear To Send	CB	5	
Data Terminal Ready	CD	20	
Data Carrier Detect	CF	8	
Transmit Clock	DB	15	(Clock From MODEM)
Receive Clock	DD	17	(Clock From MODEM)
	RS-422		
Receive Data	RD-A'	11	
	RD-B'	23	
Receive Timing	RT-A'	9	
	RT-B'	21	
Send Data	SD-A	13	
	SD-B	25	
Terminal Timing	TT-A	12	
	TT-B	24	

In a 5000IS, the first 861 has connector J3 connected to connector J4 on the 971 processor board and J2 on the 861 is connected to channel 2 on the I/O panel. Any additional 861 boards are connected in the following manner:

Board	J1	J2
Second 861	Ch. 3	Ch. 4
Third 861	Ch. 5	Ch. 6
Fourth 861	Ch. 7	Ch. 8

In a 5000SX system, the 861 boards have the following connections to the I/O panel:

Board	J1	J2
First 861	Ch. 3	Ch. 4
Second 861	Ch. 5	Ch. 6
Third 861	Ch. 7	Ch. 8
Fourth 861	Ch. 9	Ch. 10
Fifth 861	Ch. 11	Ch. 12
Sixth 861	Ch. 13	Ch. 14
Seventh 861	Ch. 15	Ch. 16
Eighth 861	Ch. 17	Ch. 18

The odd numbered channels are usually used for terminals and the even numbered channels are used for printers.

MODEL 861 MULTIPROCESSOR BOARD

Legend

JA Port A Clock Selection (Normally 1-16, 3-14 and 6-11 are shunted.)
JB Port B Clock Selection (Normally 1-4 are shunted.)
JD Reset Disable (Normally unshunted.)
JE I/O Address Selection
JF Interrupt Level Selection
J1 Serial Port 0
J2 Serial Port 1

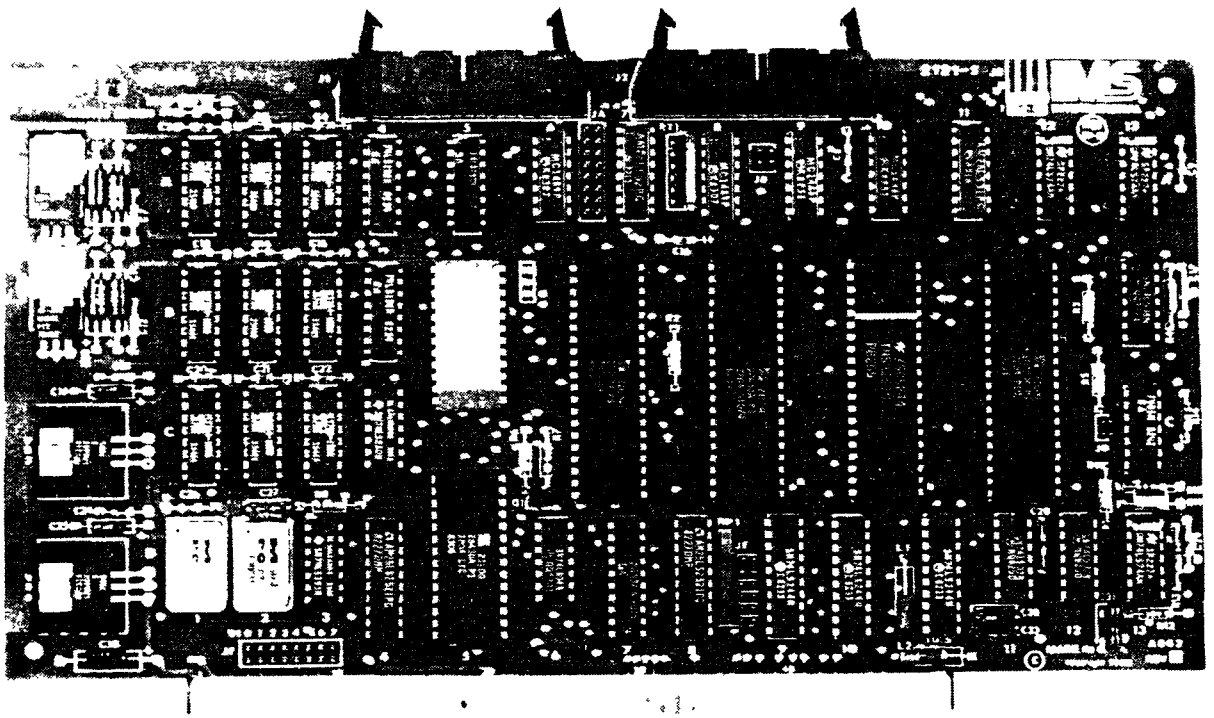


Figure 2-26
Model 861 Multiprocessor Board

2.8 FLOPPY DISK CONTROLLER BOARDS

2.8.1 MODEL 431 FLOPPY DISK CONTROLLER BOARD

The Industrial Micro Systems Model 431 floppy disk controller is used with 5-1/4" floppy drives.

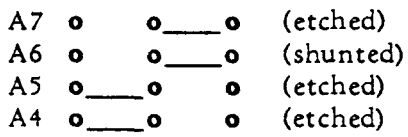
The 431 is based on the NEC uPD765 floppy disk controller chip, providing single and double density and single and double sided operation. An 8257 provides DMA operation. The 431 board can control up to four floppy drives.

CONFIGURING THE 431 BOARD

I/O Address Selection (Location JA)

The values of the most significant bits of the 431's I/O addresses are indicated by the shunts at location JA. A shunt on the right (as in A7 below) gives a "1" value to the address bit; a shunt to the left (as in A5 below) gives a "0" value to that bit. The addresses selected by the shunts below are C0H to CFH, which is the normal setting.

JA



Vectored Interrupt Level Selection (Location JB)

The JB area is used to select one of the eight vectored interrupt levels to be triggered when a floppy disk controller interrupt or a delay complete interrupt occur, depending upon the status of the interrupt mask port (OUT CCH). The pins 0-7 correspond to interrupt levels VI0-VI7, respectively.

Double Sided Drive Selection (Location JC)

The JC shunt location is used to indicate single sided (no shunt) or double sided (shunt installed) operation.

I/O ADDRESSES FOR THE 431 BOARD

C0H-C8H - 8257 DMA Controller

C0H -	Channel 0	DMA Register	
C1H -	Channel 0	Terminal Count Register	
C2H -	Channel 1	DMA Register	
C3H -	Channel 1	Terminal Count Register	
C4H -	Channel 2	DMA Register	will be reserved for
C5H -	Channel 2	Terminal Count Register	hard disk controller
C6H -	Channel 3	DMA Register	will be reserved for
C7H -	Channel 3	Terminal Count Register	2nd hard disk controller

C8H - DMA Status and Commands

C9H - NOT USED

IN CAH - NOT USED

OUT CAH - Drive select port. Data bits 0 and 1 binary weighted select one of four disk drives. All subsequent status and commands will pertain to the selected drive. These bits are latched on the board.

IN CBH - NOT USED

OUT CBH - Precisely the same significance as OUT 8AH described above.

IN CCH - Board status port. This port provides status information on the drive select, 765 interrupt and drive select delay function as follows:

DATA BIT 0 - A logical one indicates tht a 765 interrupt has occurred.

DATA BIT 1 & 2 - Binary weighted to provide the information on the drive 1, 2, or 3 is selected.

DATA BITS 3-6 - NOT USED

DATA BIT 7 - A logical one indicates that the floppy disk drive motors are on and the motor-control time-out is complete. If the motors are off or the time-out is not complete, this bit will be zero. Reading this port will start the motors and reset the thirty (30) second motor-off time-out to zero. After approximately one second this delay complete bit will be set to a logical one.

OUT CCH - Board interrupt mask. The data bits will provide information as follows:

DATA BIT 0 - A one in this position will enable a 765 interrupt on the selected vectored interrupt line. A zero disables the interrupt.

DATA BIT 1 - A one in this position enables a delay complete interrupt on the selected vectored interrupt line. Both bit 0 and 1 are latched on the board.

DATA BITS 2-7 - NOT USED

IN CDH &
OUT CDH - Precisely the same significance as IN 8CH and OUT 8CH as described above.

IN CEH - Read main status register of 765 floppy disk controller.

bit 0 = 1 Drive 0 is busy doing seek operation
bit 1 = 1 Drive 1 is busy doing seek operation
bit 2 = 1 Drive 2 is busy doing seek operation
bit 3 = 1 Drive 3 is busy doing seek operation

bit 4 = 1 Floppy disk controller is busy processing a read or write command
bit 5 Set during the execution phase of non DMA operation only
bit 6 Set if data transfer is to be from data register to processor
bit 7 Set if data register is ready to send or receive data to or from processor

IN CFH - Read disk data from data register in 765 Floppy Controller Chip.

OUT CFH - Write data for disk into data register on 765 Floppy Controller Chip.

CONNECTIONS

The J1 connector on the 431 board is connected to the floppy disk drive with a ribbon cable. If there is more than one drive, this cable is daisy-chained to the other drive(s). The pin assignments for the ribbon cable are Shugart compatible. They are listed below. The pin numbers are the same for the board and the drive because a flat ribbon cable is used.

Pin	Signal
2	SPARE
4	IN USE
6	SEL 4
8	INDX
10	SEL 1
12	SEL 2
14	SEL 3
16	MON
18	IN
20	STP
22	WDAT
24	WGAT
26	TRACK0
28	WPROT
30	RDATA
32	SDE1
34	SEPDAT
36	-
38	-
40	-
42	-
44	-
46	-
48	-
50	-
ALL ODD	GROUND

MODEL 431 5" FLOPPY DISK DRIVE CONTROLLER BOARD

Legend

JA Address Selection. Normally A7 and A6 are shunted to the right and A5 and A4 are shunted to the left.

JB Vector Interrupt Level selection.

JC Double-sided Drive selection.

J1 Connector to floppy disk drive.

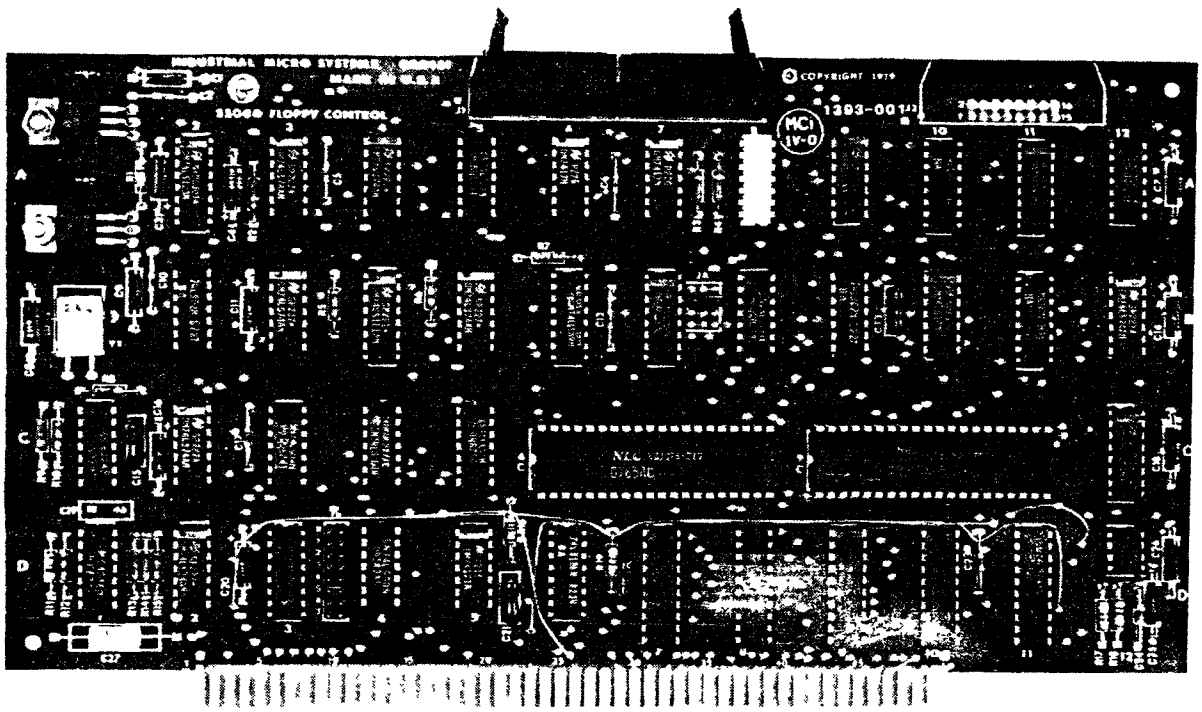


Figure 2-27
431 5" Floppy Disk Drive Controller Board

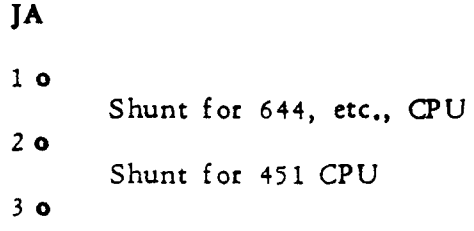
2.8.2 MODEL 930 FLOPPY DISK CONTROLLER BOARD

The 930 board is a floppy disk drive controller which can be used with either 5" or 8" disk drives. A single 930 board can control up to four drives of the same size.

CONFIGURING THE 930 BOARD

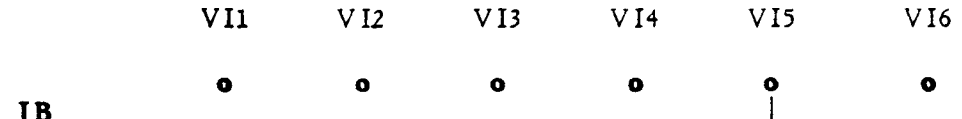
Processor/DMA Control (Location JA)

During a DMA cycle, bus control is transferred between the 930 Floppy Disk Controller and the CPU. IMS uses two different methods of transfer, dependent on the CPU. The shunt block JA should have pins 2 and 3 (lower 2 pins) connected when the system CPU is an IMS Model 451; pins 1 and 2 (upper 2 pins) should be connected for all other IMS CPU's.



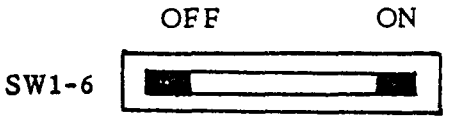
Vectored Interrupt Level Selection (Location JB)

The Vectored Interrupt Level of the 930 is etched to be VI5. This etch may be cut and, by means of a shunt, the 930 may be connected to any input, VI1 through VI6.



I/O Base Address Selection (SW1-6)

Switch 6 on the package at location 1D assigns the I/O addresses for the 930 board. This switch should be on for 8" floppy disk drives, resulting in I/O address 80H to 8FH. For a system with 5" floppy disk drives, switch 6 should be off, resulting in I/O addresses C0H to CFH.



Program/Drives I/O Switches (SW1)

Switches 1 through 4 on the DIP at location 1D can be read by the program and are used to identify the type of drive connected to the controller. Switch 2 is used by the hardware and must be "on" for 8 inch drives. Switches 1 through 4 are read by the program as Data Bits 7 through 4; an "on" switch is read as a zero. The settings for all the switches in the package are shown below for different types of drives.

SW1

	Drive Type	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6	SW1-7	SW1-8
1	8" SS	on	on	on	off	off	on	off	on
2	8" DS	on	on	off	on	off	on	off	on
3	5" DS 96 TPI	on	off	on	off	on	off	off	on
4	5" DS 48 TPI	on	off	off	on	on	off	off	on
5	5" SS 48 TPI	on	off	off	off	off	off	off	on
6*	5" DS ?? TPI	on	off	on	on	on	off	off	on

(SS - single sided, DS - double sided, TPI = tracks per inch)

*Controllers shipped loose will be set in this configuration. This setting allows 48 or 96 TPI and slow step rates.

CONNECTIONS

If the 930 board is used to control 5" disk drives, the J2 connector is connected to the disk drives in a daisy-chain. If the system contains 8" drives, then the J1 connector is daisy-chained to the drives. The signals for each connection are listed below. Flat ribbon cables are used to make the connection.

Pin	8 Inch Drives J1 (50 Pins)	5 Inch Drives J2 (34 Pins)
2	low write current	--
4	--	--
6	--	select 4
8	--	index
10	2 sided	select 1
12	disk change	select 2
14	side 1	select 3
16	--	motor on
18	head load	in
20	index	step
22	--	write data
24	--	write gate
26	select 1	track 0
28	select 2	read data
30	select 3	side 1
32	select 4	--
34	in	--
36	step	
38	write data	
40	write gate	
42	track 0	
44	write protected	
46	read data	
48	--	
50	--	
All odd pins	ground	ground

MODEL 930 FLOPPY DISK DRIVE CONTROLLER BOARD

Legend

JA Processor/DMA Control.
JB Vector Interrupt Level Selection.
SW1 Drive Identification Switches.
J2 Connector to Floppy Disk Drives.

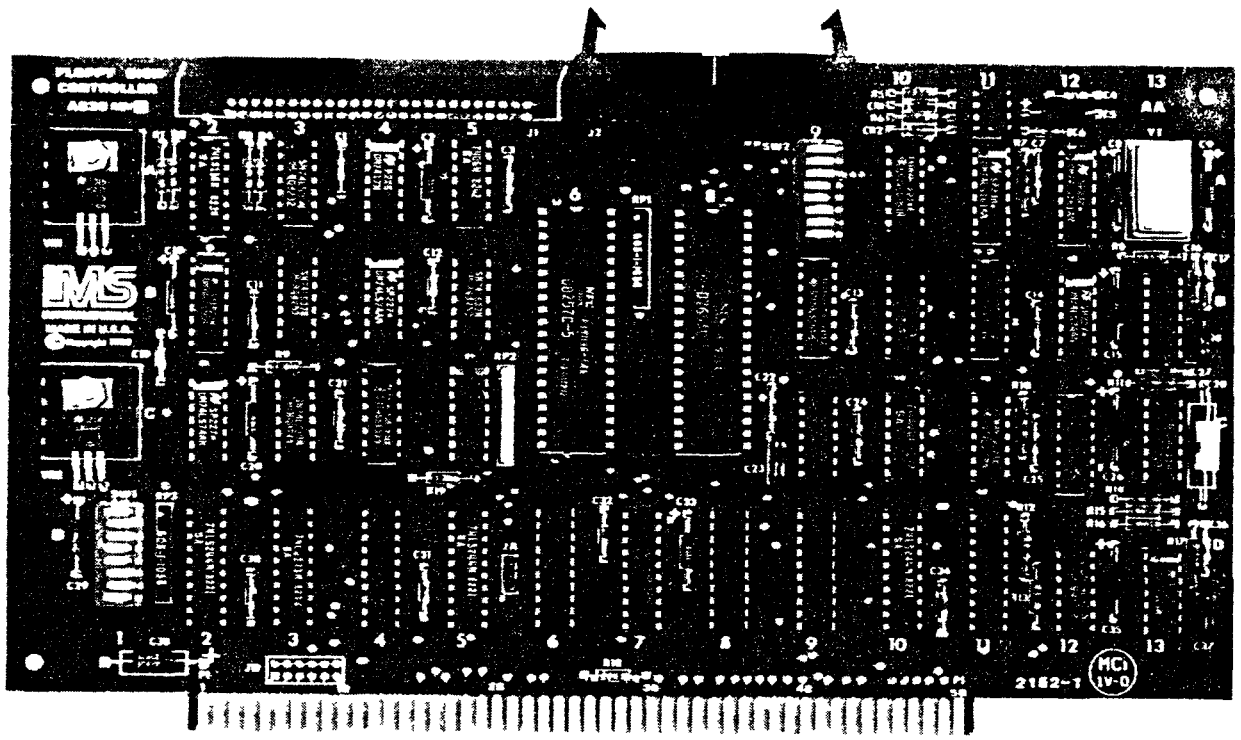
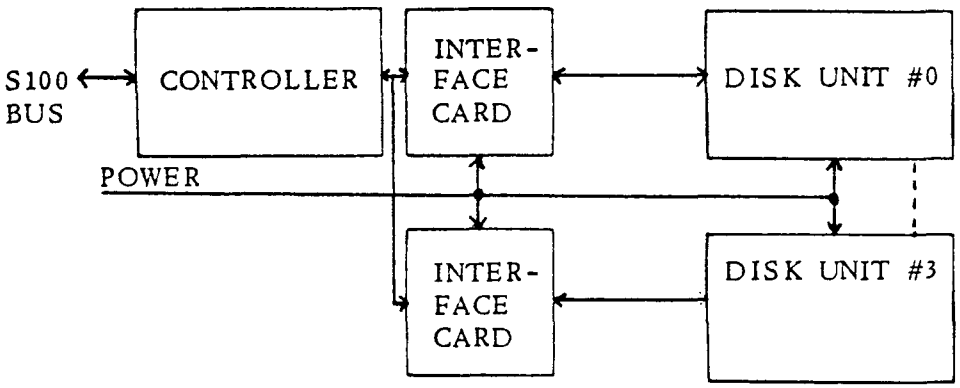


Figure 2-28
930 Floppy Disk Drive Controller Board

2.9 5¼" WINCHESTER DISK DRIVE SUBSYSTEM

GENERAL DESCRIPTION

The disk subsystem consists of the controller, up to 4 disk units, a disk interface card for each disk unit, together with power and control cables, as shown below:



The function of the controller is to transfer data between the bus and the disk units. The interface card provides sector signals to the controller and also decodes the drive select signals.

DISK DRIVE

The disk unit is a 5¼ inch Winchester Technology sealed fixed disk drive with typical specifications as follows:

Environment:	Ambient Temperature	10^{o} to 50^{o} F.
	Relative Humidity	10% to 80% (non-condensing)
Power:	+12VDC ±10%, 2A typical, (4A during motor start)	
	+5VDC ±5%, 0.65A typical	
Unformatted Capacity:	10.4 kilobytes per track	
Transfer Rate:	5.0 Megabits per second	
Access Time:	18 milliseconds track to track seek (including settling time) 90 milliseconds average seek 215 milliseconds maximum seek 8.3 milliseconds average rotational latency	

CONNECTIONS

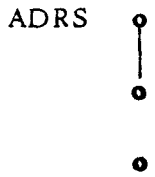
The connector on the upper edge of the 821 controller card is daisy-chained with all of the interface cards. Each interface card is attached to a Winchester drive.

CONFIGURING THE 821 WINCHESTER CONTROLLER BOARD

Address Selection (Pad ADRS)

The upper pair is connected for 5" drives, setting the board address to A0H. This connection is etched.

The lower pair is shunted for 8" drives, which sets the board address to A8H.

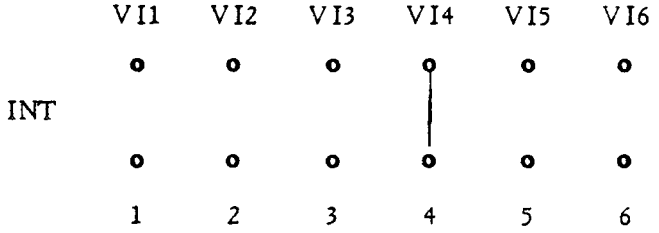


ECC Test Option (Pad ECC)

Normally, the upper pair is shunted. The lower pair is shunted for use with the TESTECC command in the test program.

Interrupt Level Selection (Pad INT)

Installation of a shunt selects the interrupt level for the controller. Normally, VI4 is etched.



MODEL 821 WINCHESTER CONTROLLER BOARD
STANDARD CONFIGURATION

Legend

ADRS	5" etched	Sets board address to A0H
	8" shunt upper pair	Sets board address to A8H
ECC	RUN	Used with TESTECC command in test program. Normally in run position.
INT	etched	Set to VI4 interrupt.

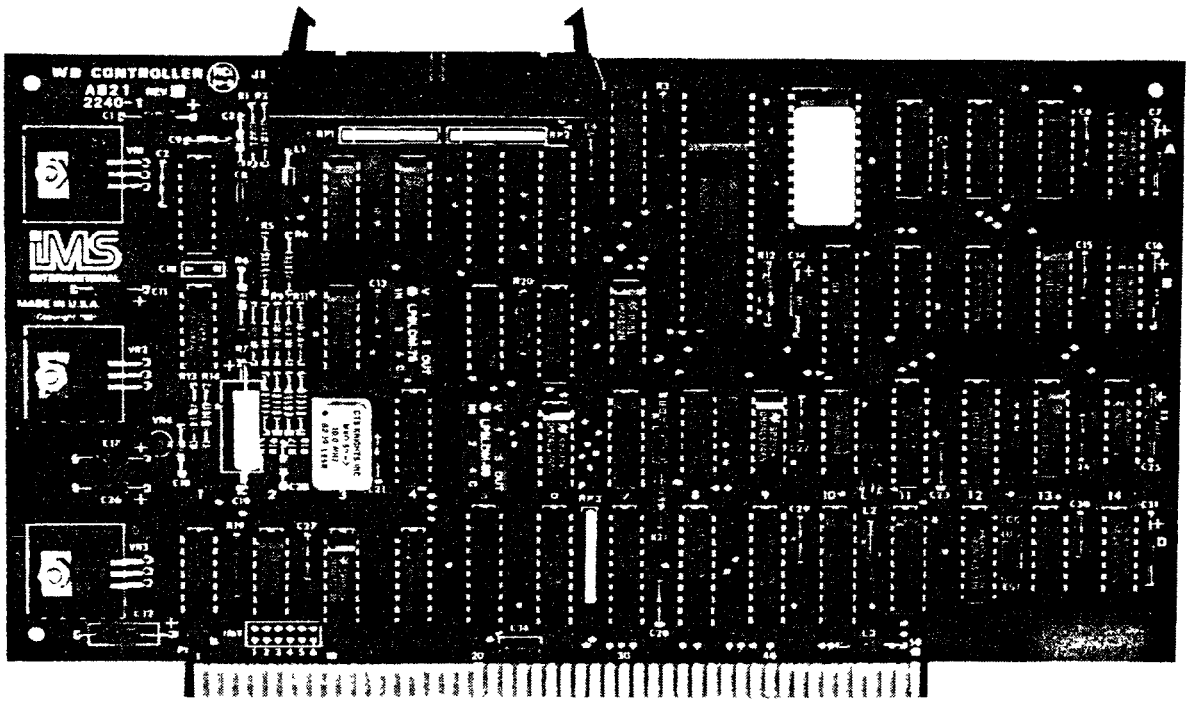


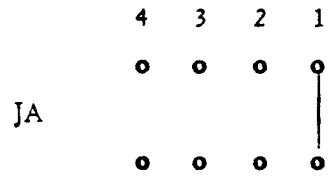
Figure 2-29
Model 821 Winchester Controller Board

CONFIGURING THE 900 WINCHESTER INTERFACE BOARD

Drive Select (Location JA)

A shunt is installed to indicate the drive number. 1 is shunted for drive #1, 2 is shunted for drive #2, etc.

Normally, there is only one Winchester drive, so 1 would be shunted.



Terminating Resistor Pack (Location RP2)

The 760-5-R220/330 resistor pack is removed on every interface card except the one for the last drive. Normally, there is only one Winchester drive so the resistor pack would stay in.

Figure 2-30
Winchester Interface Card

2.10 MODEL 662 VIDEO DISPLAY BOARD

The 662 Video Display Board is used in the IMS 5000IS. It receives data from the keyboard and transmits it to the processor. It also controls the CRT, with the ability to emulate four current CRT terminals. It has an RS-232 serial port and an RS-422 port.

SPECIFICATIONS

Processor:	8085 microprocessor
ROM Capacity:	8 Kbytes
ROM Type:	2732 or equivalent EPROM
RAM Capacity:	8 Kbytes
RAM Type:	6116 2K x 8 static RAMs
Keyboard Interface:	Asynchronous, TTL level serial input, 50-9600 baud, +5V mark bit, sync bit, 8 data bits and 1 stop bit. Single line active high output for controlling bell on keyboard.
Monitor Interface:	TTL level interface signals with either active-high or active-low sync signals available. Horizontal sweep rate is 19.4KHz at 60Hz and 18KHz at 50Hz. Video bandwidth should be >20MHz.
Screen Format:	24 lines (plus status line) by 80 columns, 7 x 8 characters with 2 descenders in a 9 x 12 matrix.
Power Requirements:	+ 5 volts @ 800ma +12 volts @ 30ma -12 volts @ 20ma
Operating Environment	0-55 deg. C.

CONFIGURING THE 662 BOARD

RS-232/RS-422 Mode Selection (JA)

Shunt JA indicates whether RS-232 or RS-422 protocol is being used. RS-422 is used when the 662 board is used in a terminal which is far away from the computer. In a 5000IS system, this location always has the upper pair shunted.

JA

RS-232C -- shunt 1-2
RS-422 -- shunt 2-3

Vertical SYNC Polarity (JC)

The shunt on JC selects the polarity of the vertical SYNC signal to the monitor. If pins 1 and 2 are shunted, VSYNC has minus polarity; if 2 and 3 are shunted, VSYNC has plus polarity.

JC
1 o
2 o
3 o

Horizontal SYNC Polarity (JB)

The shunt on JB selects the polarity of the horizontal SYNC signal. Pins 1 and 2 shunted indicates minus polarity; if 2 and 3 are shunted, HSYNC has plus polarity.

JB
1 o
2 o
3 o

Character Generator Selection (JD)

This location indicates the type of EPROM used for character generation. Normally, the shunts are set up for a 2716 EPROM (2 Kbytes).

JD		
1 o	2716 EPROM --	1-2 shunted
2 o		4-5 shunted
3 o		
4 o	2732 EPROM --	1-2 shunted
5 o		3-4 shunted

SW-1 to SW-4)

The first four switches on the switch package SW1 select the baud rate used when the system is first powered up. The baud rate is selected in the following manner:

	SWITCH #			
Baud	1	2	3	4
19,200	ON	ON	ON	ON
9,600	OFF	ON	ON	ON
4,800	ON	OFF	ON	ON
2,400	OFF	OFF	ON	ON
1,800	ON	ON	OFF	ON
1,200	OFF	ON	OFF	ON
600	ON	OFF	OFF	ON
300	OFF	OFF	OFF	ON
150	ON	ON	ON	OFF
110	OFF	ON	ON	OFF

Cursor Options (SW1 - 5,6)

The cursor's characteristics at power-up are determined by switches 5 and 6 of switch pack SW1. If switch #5 is on, the cursor is a reverse block, if switch #5 is off, the cursor is an underline. When switch #6 is on, the cursor blinks, otherwise it is solid.

Status Line Selection (SW1-7)

If switch #7 of SW1 is on, then the status line will be displayed at power-up as the 25th line on the screen. If switch #7 is off, the status line will be displayed at power-up, but the depression of any key will cause it to disappear.

Frequency Selection (SW1-8)

Switch #8 of SW1 is on for 60 Hz machines and off for 50 Hz machines.

Transmission Characteristics (SW2-1,2,3,4,5,6)

The first six switches on switch pack SW2 select the transmission characteristics for the console.

Switch #1	ON -	A 7 bit word is transmitted
	OFF -	An 8 bit word is transmitted
Switch #2	ON -	No modem control
	OFF -	Modem control
Switch #3	ON -	1 stop bit
	OFF -	2 stop bits
Switch #4	ON -	No parity
	OFF -	Enable parity
Switch #5	ON -	Odd parity
	OFF	Even parity
Switch #6	CN -	Mark (Stick Parity). This switch indicates that the parity bit will always be the same value. This switch should be ON only when switch #1 is ON and switch #4 is ON.

Power-Up Operating Mode Selection (SW1-7,8)

Switches 7 and 8 on SW2 select the operating characteristics used at power-up. If switch #7 is ON, the console will be in the IMS "Native" mode at power-up. If switch #7 is OFF, the console emulates the Televideo 950 terminal at power-up. Switch #8 selects full or half duplex transmission: on for full duplex and off for half duplex.

The switch settings for SW1 and SW2 are summarized below:

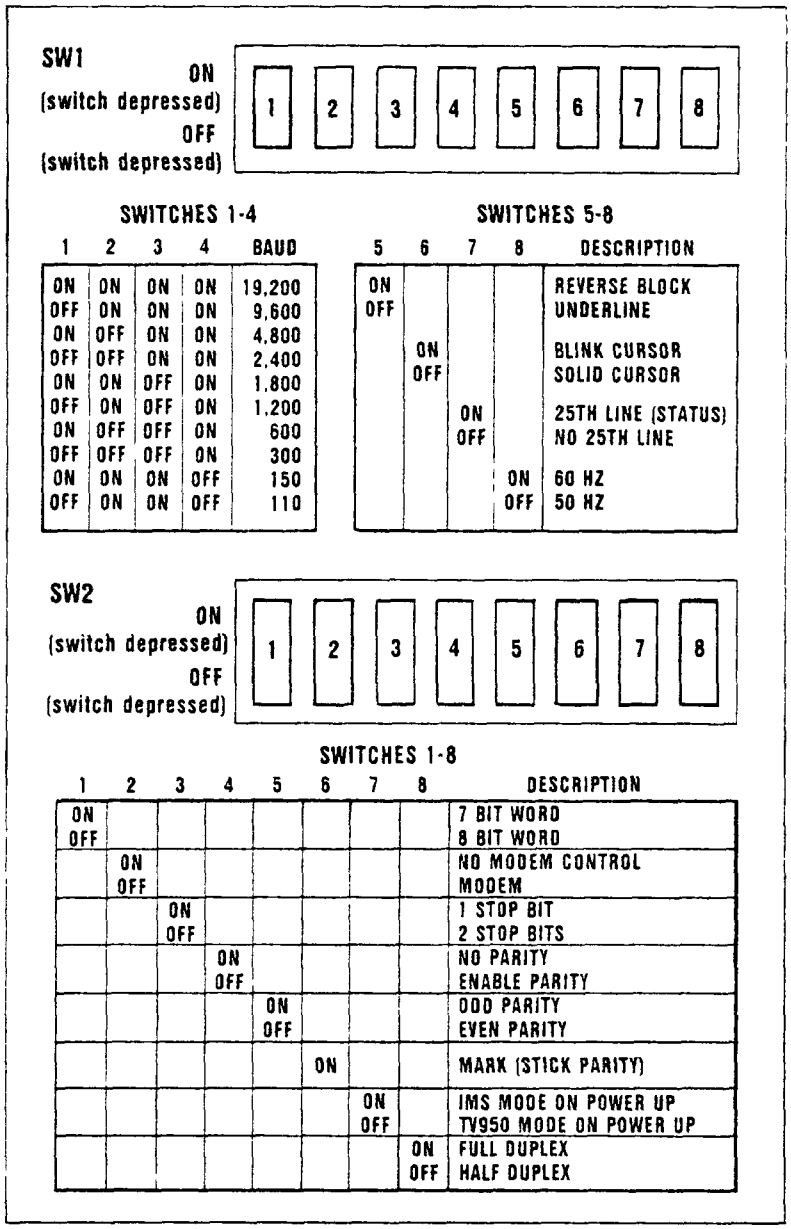


Figure 2-31
662 Board Switch Settings

662 BOARD CONNECTIONS

Keyboard Connection (J1)

Connector J1 on the upper edge of the 662 board is connected to the detachable keyboard via a plug on the bottom of the 5000IS. The signals are as follows:

pin	1	. . . . +12 volts
pin	2	. . . . +12 volts
pin	3	. . . . GND
pin	4	. . . . Bell output
pin	5	. . . . GND
pin	6	. . . . Keyboard serial data

Modem Connection (J2)

This connection is not used in the 5000IS.

Monitor Connector (J3)

Connector J3 on the lower edge of the 662 board is connected to the keyboard interface card (890) which is connected to the CRT monitor board. J3 has the following pin assignments:

pin	1	. . . . GND
pin	2	. . . . Vertical SYNC
pin	3	. . . . VIDEO
pin	4	. . . . GND
pin	5	. . . . Horizontal SYNC
pin	6	. . . . NOT USED
pin	7	. . . . Keyboard serial data
pin	8	. . . . Keyboard bell output
pin	9	. . . . NOT USED
pin	10	. . . . GND

Power Supply Connection (J4)

Connector J4 on the lower right edge of the 662 board is connected to connector J5 on the power supply. The pin assignments for J4 are listed below:

pin	1	. . . . GND
pin	2	. . . . GND
pin	3	. . . . -12 volts
pin	4	. . . . +12 volts
pin	5	. . . . +5 volts
pin	6	. . . . +5 volts

TTL Compatible Communications Connector (J5)

Connector J5 is located in the center of the lower edge of the 662 board. It is connected to socket J3 on the 971 processor board. The pin assignments are below:

pin 1 . . . . Receive Data
pin 2 . . . . GND
pin 3 . . . . Transmit Data

Graphics Adapter Connection (J6)

Connector J6 connects to the IMS graphics board to add graphic capability to the console. The pin assignments are listed below:

pin 1 . . . . GOSC+
pin 2 . . . . GND
pin 3 . . . . VSYNC+
pin 4 . . . . GND
pin 5 . . . . HSYNC+
pin 6 . . . . GND
pin 7 . . . . HGLT+
pin 8 . . . . GND
pin 9 . . . . EHSYNC-
pin 10 . . . . GND
pin 11 . . . . CHDOTS+
pin 12 . . . . GND
pin 13 . . . . DISPG+
pin 14 . . . . GND
pin 15 . . . . KBUZ-
pin 16 . . . . KSD+

Reset Connector (J7)

This connector, located near the center of the upper edge of the board, can be used to reset the 662 board. It is normally not used.

pin 1 . . . . External Reset In
pin 2 . . . . GND

Light Pen Connector (J8)

The 662 board can be connected to a light pen via connector J8. Normally, no connection is made. The pin assignments are as follows:

pin 1 . . . . +5 volts
pin 2 . . . . GND
pin 3 . . . . Pen down (-)
pin 4 . . . . Light strobe (-)

MODEL 662 VIDEO DISPLAY BOARD

Legend

1. J1 Keyboard Connector
2. J2 Modem Connector
3. J3 Monitor Connector
4. J4 Power Connector
5. J5 TTL Compatible Communications Connector
6. J6 Graphics Adapter Connector
7. J7 Reset Connector
8. J8 Light Pen Connector
9. JA RS-232C/RS-422 Mode Selection Shunt
10. JB Horizontal SYNC Polarity Selection Shunt
11. JC Vertical SYNC Polarity Selection Shunt
12. JD Character Generator Selection
13. Contrast Control Potentiometer
14. SW2 Terminal parameter switch 1
15. SW1 Terminal parameter switch 2

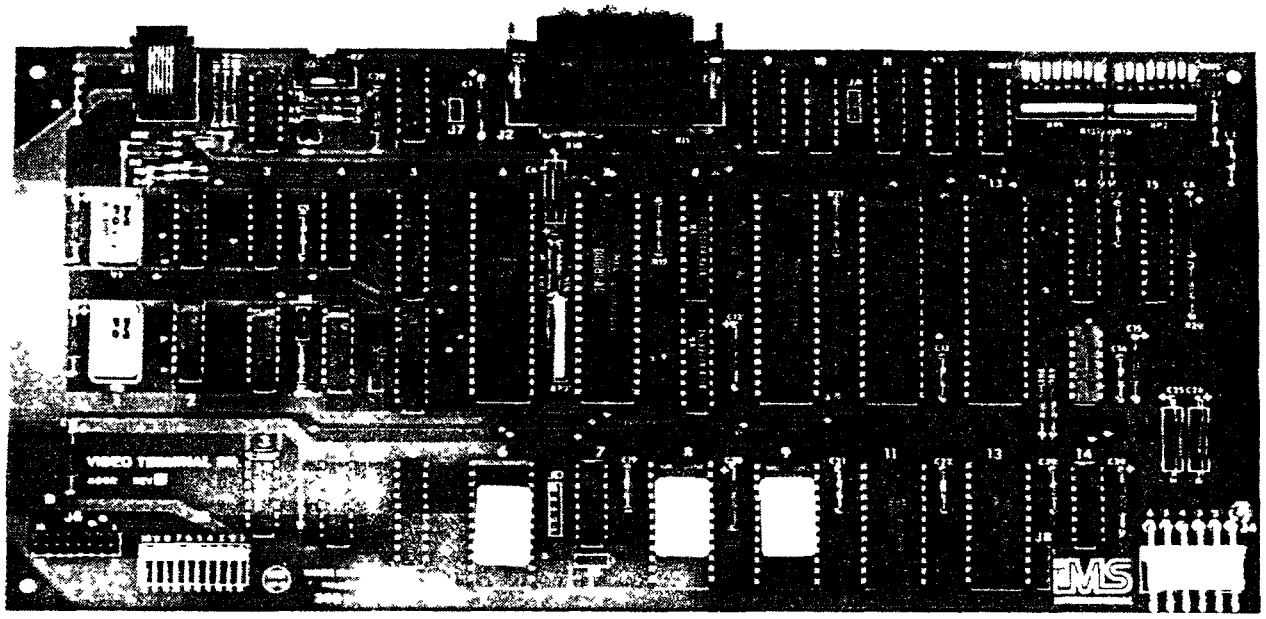


Figure 2-32
Model 662 Video Display Board

SECTION 3

Disk Drives and Tape Cartridge Unit

INTRODUCTION

This section will cover the standard shunting, cabling and basic specifications of the floppy, Winchester, and tape drives used in the 8000 Series systems.

The floppy drives used in 5000 Series systems are TEAC 5¼" half width drives. The Winchester drive used is one of the Rodime RO-200 Series 5" drives. You may also have a stand-alone tape cartridge unit, which is manufactured by Digidata.

3.0 TEAC FD-55 FLOPPY DISK DRIVE

The TEAC floppy disk drives are storage devices which use a standard removable 5¼" flexible diskette as a storage medium.

They are capable of supporting either single density format (FM), or double-density format (MFM) and double sided recording. The TEAC FD-55F has 96 tracks per inch; the FD-55B has 48 tracks per inch.

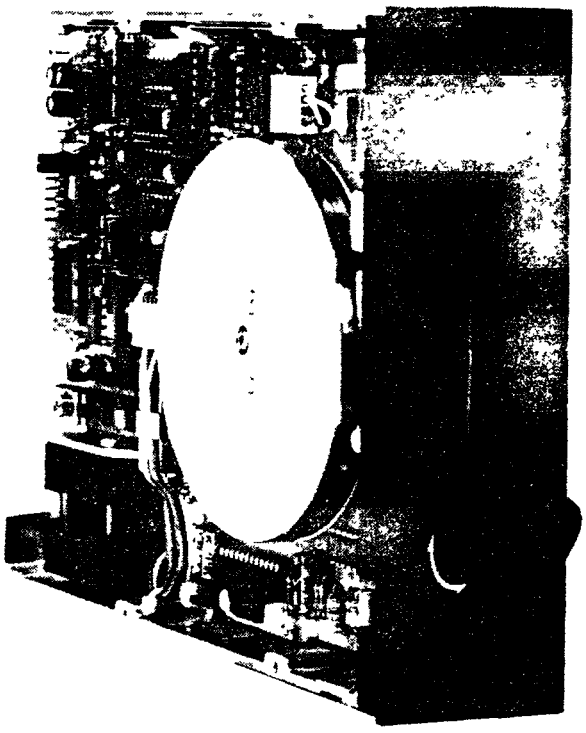


Figure 3-1 TEAC 5¼" Floppy Disk Drive

SPECIFICATIONS

Physical Dimensions	
Width	5.75" nominal
Height	1.63"
Depth	7.99"
Weight	3.31 lbs.

Electrical Specifications	
+12V DC power	+12V ±5%, 0.25A typical
+5V DC power	+5V ±5%, 0.5A typical

Environmental Conditions	
Operating temperature	4°C to 46°C (40°F to 115°F)
Storage temperature	-22°C to 60°C (-8°F to 140°F)
Wet bulb temperature	29°C (84°F) maximum
Operating humidity	20% to 80% non-condensing

Operational Characteristics	
Number of tracks/disk	160
Track to track access time	less than 3 ms
Head settling time	less than 15 ms
Average access time (including settling time)	94 ms
Motor start time	less than 400 ms
Disk rotational speed	300 rpm
Instantaneous speed variation	less than ±1.5%

Recording Method	FM	MFM
Data Transfer rate (K bits/sec)	125	250
Tracks/disk	160	160
Innermost track bit density (bpi)	2,961 (side 1)	5,922 (side 1)
Innermost track flux density (frpi)	5,922 (side 1)	5,922 (side 1)
Data Capacity		
Unformatted		
K bytes/track	3.125	6.25
K bytes/disk	500	1,000
Formatted (16 sectors/track)		
K bytes/track	2.048	4.096
K bytes/disk	327.68	655.36

Reliability

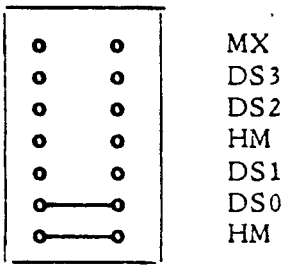
Mean time between failures (MTBF)	10,000 power on hours or more (for typical usage)
Mean time to repair (MTTR)	30 minutes
Error Rates	
Soft read error	1 per 10^9 bits (up to 2 retries)
Hard read error	1 per 10^{12} bits
Seek error	1 per 10^6 seeks

Shunting

On the side of the floppy disk drive is a circuit board (Figure 3-2) which is supplied by TEAC. The shunt options on the board are explained below.

Drive Select

There should be a shunt that indicates the drive number, DS0, DS1, DS2 or DS3. If your system has two drives, one would have a shunt on DS0 and the other would have a shunt at DS1. If the system has only one floppy disk drive, DS0 would be shunted.

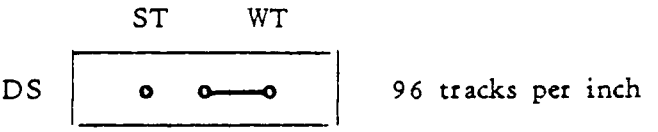


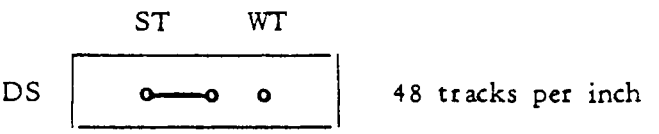
Terminating Resistor

If your system has more than one drive, the 330 Ω ±5% terminating resistor should be removed from all but the last drive. For example, if your system had only one drive, the terminating resistor would stay in. If your system had two drives, the terminating resistor would be removed from the drive shunted as DS0 and kept in the drive shunted DS1.

Track Density

The number of tracks per inch is indicated on the DS shunt. For 96 t.p.i. drives, the WT side is hunted; for 48 t.p.i. drives, the ST side is shunted.





Legend

1. Drive Select Shunt
2. Terminating Resistor
3. Track Density Shunt

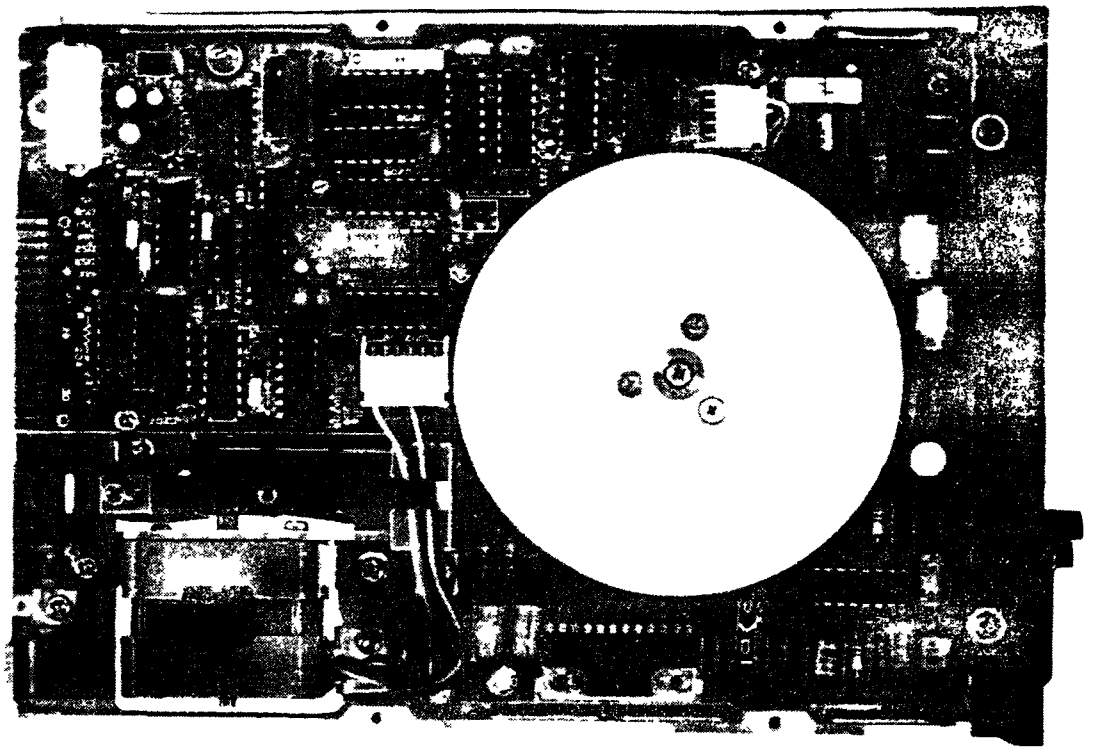


Figure 3-2
TEAC Floppy Disk Drive Board

Cabling

The I/O lines are 'daisy-chained' from one floppy drive to another, using a flat ribbon cable. Each drive has a separate cable going to the power supply. The cabling is shown below.

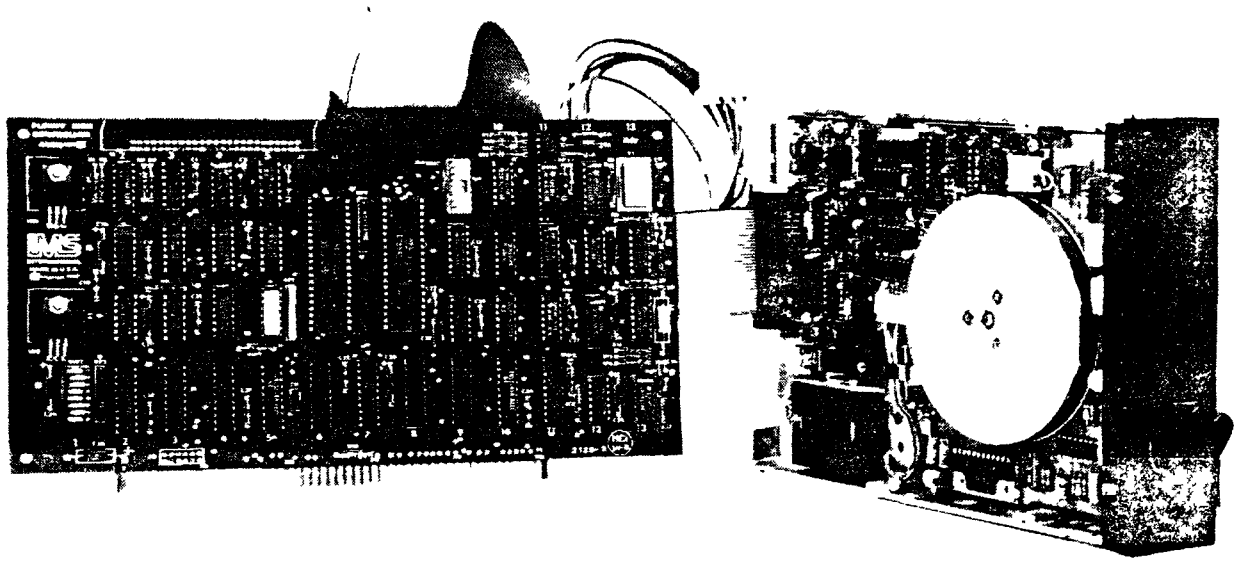


Figure 3-3
TEAC Floppy Disk Drive Cable Diagram

3.1 RODIME RO 200 SERIES WINCHESTERS

The Rodime RO 200 series of 5¼ inch (130 mm) Winchester disk drives provide fast access data storage for use with small business computers, terminals and microprocessor based systems. There are four models in the series, RO 201, RO 202, RO 203, and RO 204, containing 1, 2, 3 and 4 magnetic disks respectively and ranging in total data storage from 6 to 24 megabytes.

A summary of the important performance parameters is given below:

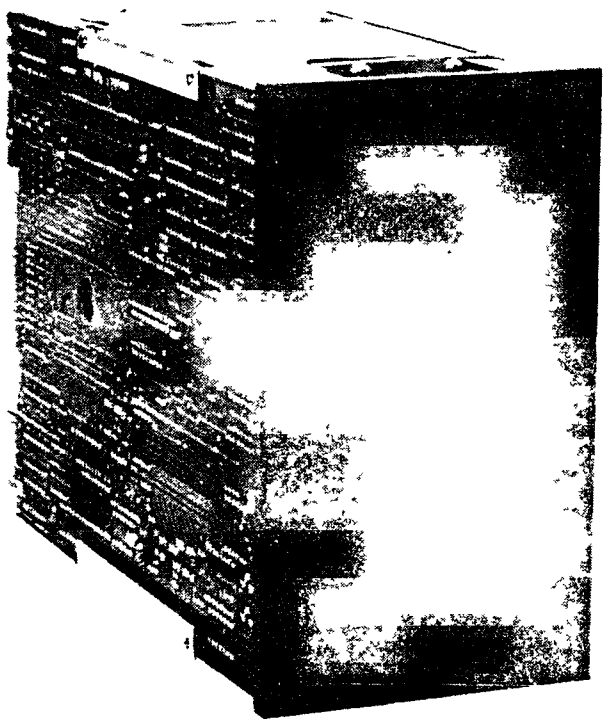


Figure 3-4 Rodime 5¼" Winchester Disk Drive

SPECIFICATIONS

Models: RO201, 202, 203, 204

Number of Disks	1,2,3,4
Number of Heads	2,4,6,8
Unformatted capacity	6.67, 13.33, 20.00, 26.67 Mbytes
Formatted capacity (typical)	
per drive (M bytes)	5.89, 11.79, 17.69, 23.59 Mbytes
per track (bytes)	9216 bytes
per sector (bytes)	512 bytes
Sectors per track	18
Cylinders	320
Transfer rate	5 Mbits/second
Seek times (ms) (including settling)	
track to track	18 ms
average	90 ms
maximum	215 ms
Average latency	8.3 ms
Flux reversals per inch	8900 (max)
Tracks per inch	356
Rotational speed	3600 rpm
Power requirements	5V DC (±5%) at 0.65A typical 12V DC (±10%) at 2A typical (4A motor start)
Dimensions	8.00 x 5.75 x 3.25 inches
Operating Environment	10°C to 50°C 10% RH to 85% RH (non-condensing)
Vibration	
Operating	.006 inch displ., 5-60 Hz 1g pk accin., 60-500 Hz
Non-operating	.040 inch displ., 5-30 Hz 2g pk accin., 30-500 Hz

Shock	
Operating and non-operating (without transit lock)	3g pk, less than 10 ms max 2 per second.
Non-operating (with transit lock)	20g pk, less than 20 ms, max 1 per 10 second
Interface	ST506 variant of SA1000
Indicators	Two red LED's fixed to the master electronics board are visible through the facia when they are illuminated. The "Power-On" LED is on when the drive is READY with no error condition present. It is also used to indicate fault conditions in the drive. The "Select" LED is on when the drive is selected by the host provided the "Power-On" LED is on. The "Power-On" LED is positioned closest to the center of the facia. Note that this LED will not come on if the condition 2.5.1, 5V risetime, is not met since the microprocessor will not receive an initial reset.

Fault Finding, Front Panel Fault Codes

The "Power-On" LED is used to flash error messages should certain fault conditions arise on the drive. A four bit binary code is used (long flash = logical 1, short flash = logical 0) with the most significant bit occuring first:

e.g. short, short, long, short = 2 (0010)

Fault Code	**1**	(0001)	No index track data burst.
Fault Code	**2**	(0010)	No Flag 00
Fault Code	**3**	(0011)	Motor speed outside ±1% tolerance in normal operation.
Fault Code	**4**	(0100)	Motor speed outside ±10% tolerance in normal operation.
Fault Code	**5**	(0101)	Flag 00 stays TRUE.
Fault Code	**6**	(0110)	STEP received while WRITE GATE is TRUE.
Fault Code	**7**	(0111)	Static WRITE FAULT.
Fault Code	**8**	(1000)	Not used.
Fault Code	**9**	(1001)	Microprocessor self-test fail.
Fault Code	**10**	(1010)	No index.
Fault Code	**11**	(1011)	Motor not up to speed.

Fault codes 1, 2, 3, 5, 9, 10 and 11 are monitored during the initial power-up sequence of the drive. The remaining codes, namely 4, 6 and 7 are constantly monitored during normal operation. All fault codes are latched by the processor and the drive must be restarted to clear. Codes 3, 4, 10 and 11 generate an interface WRITE FAULT as do those fault conditions leading to code 7. If one of these codes if flashed, maintenance personnel should be called.

Cabling

The Winchester drive itself is connected to the power supply and a small interface card. The interface card is connected to the 821-5 Winchester Controller Board. If you had more than one Winchester drive, the I/O cable would be daisy-chained between the interface cards for each Winchester.

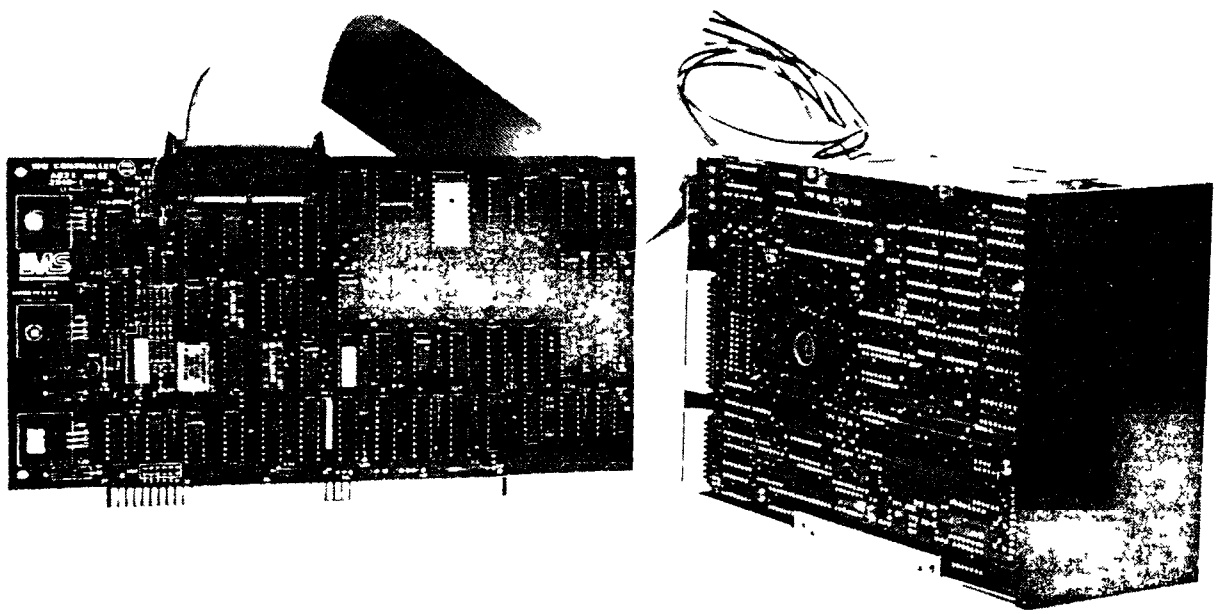


Figure 3-5
Rodime Winchester Drive Cable Diagram

3.2 TAPE CARTRIDGE SYSTEM

GENERAL DESCRIPTION

The IMS Tape Cartridge System permits the transfer of programs and data files from a Winchester disk to an easy-to-handle tape cartridge, facilitating off premises data storage and shipping. Data written to the tape is written in 8208 byte blocks, allowing a full 8K data record with a 16 byte file control block. This configuration allows 13.4 megabytes of formatted storage on a 450 foot, ¼" tape. Data is written sequentially on each track, and the tape is rewound and the next track selected as each track is filled. The tape cartridge system consists of an S-100 controller (DS100) board, a 6400 BPI cartridge tape drive, power supply, and cables.

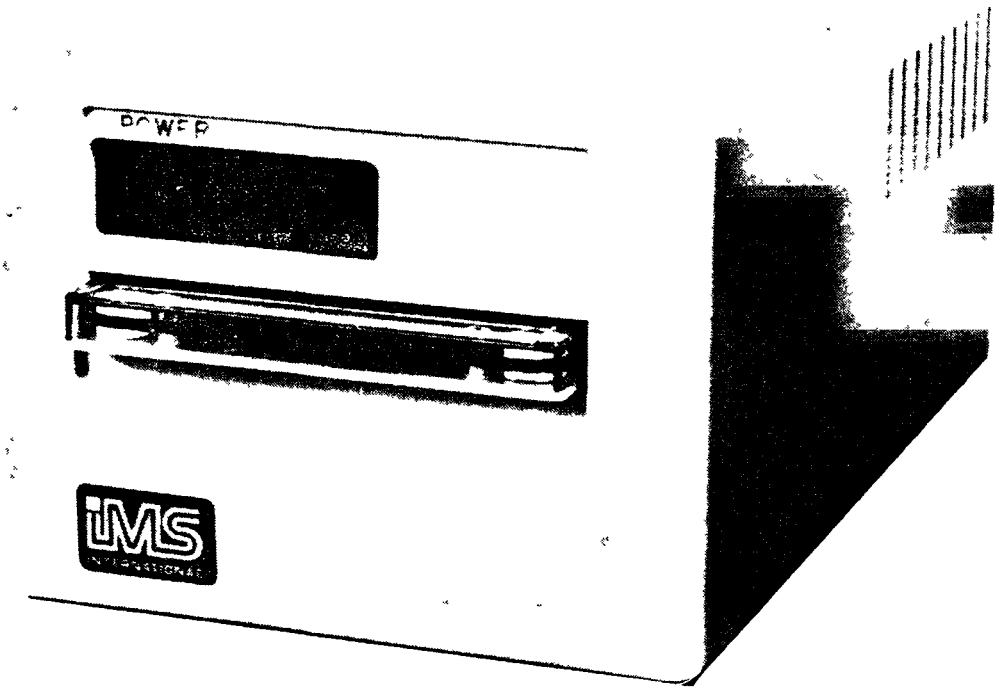


Figure 3-6
Stand-Alone Tape Cartridge System

SPECIFICATIONS

Physical Dimensions

Width	6.95" max
Height	4.25" max
Depth	7.25" max
Weight	3.2 lbs. max

Operating Environment

+5° to +45°C, cartridge limited
20% to 80% relative humidity, non-condensing

Non-Operating Environment

-30° to +60°C, hardware
+5° to 45°C, cartridge storage
-40° to +45°C, cartridge storage
20% to 80% relative humidy, non-condensing

Performance Specifications

Cartridge type	Per ANSI X3.55 - 1977 Specifications, 300 or 450 ft. length
Recording density	6400 bpi (MFM)
Tape speed, synchronous	30 ips forward and reverse
Tape speed, search	90 ips ±5%, long term forward and reverse
Speed variation, synchronous (maximum)	±3% long term (including cartridge effects) ±7% short term (including cartridge effects)

(measured per ANSI/ECMA/ISO standards)

Rewind time	60s nominal for 450' length of tape
Disk rotational speed	300 rpm

Instantaneous speed variation - less than ±1.5%

CONTROLLER

The cartridge tape controller has a 4 switch package which selects the I/O port address. The values for different settings are shown below. The standard I/O address used by IMS is D0-DF.

Switch Number	Switch Value	I/O Addresses	SW1	SW2	SW3	SW4
SW1	80	00 - 0F	OFF	OFF	OFF	OFF
SW2	40	10 - 1F	OFF	OFF	OFF	ON
SW3	20	20 - 2F	OFF	OFF	ON	OFF
SW4	10	30 - 3F	OFF	OFF	ON	ON
		40 - 4F	OFF	ON	OFF	OFF
		50 - 5F	OFF	ON	OFF	ON
		60 - 6F	OFF	ON	ON	OFF
		70 - 7F	OFF	ON	ON	ON
		80 - 8F	ON	OFF	OFF	OFF
		90 - 9F	ON	OFF	OFF	ON
		A0 - AF	ON	OFF	ON	OFF
		B0 - BF	ON	OFF	ON	ON
		C0 - CF	ON	ON	OFF	OFF
Standard IMS Setting ⟶		D0 - DF	ON	ON	OFF	ON
		E0 - EF	ON	ON	ON	OFF
		F0 - FF	ON	ON	ON	ON

Figure 3-7
Switch Settings - Cartridge Tape Controller

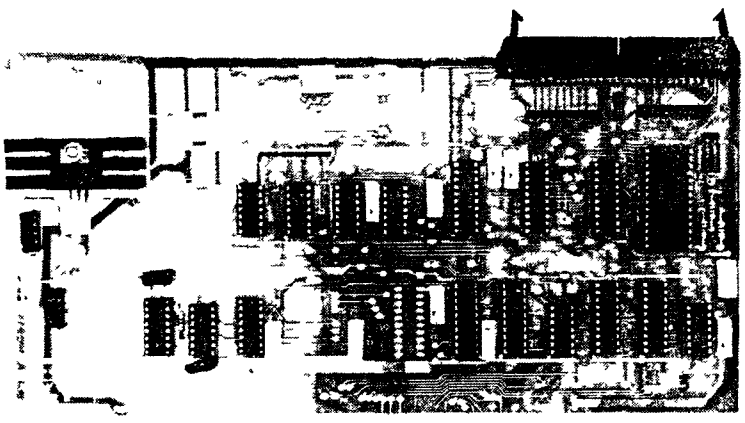


Figure 3-8
Tape Cartridge System Controller Board

RECORDING DETAILS

The cartridge tape unit records data serially on a track that stretches from one end of the tape to the other. When this track is filled up, the tape rewinds and the next track is filled in the same manner. There are four tracks, resulting in 17.3 megabytes of unformatted storage (14.3 Mb formatted) on a 450 foot tape. The format used is shown below.

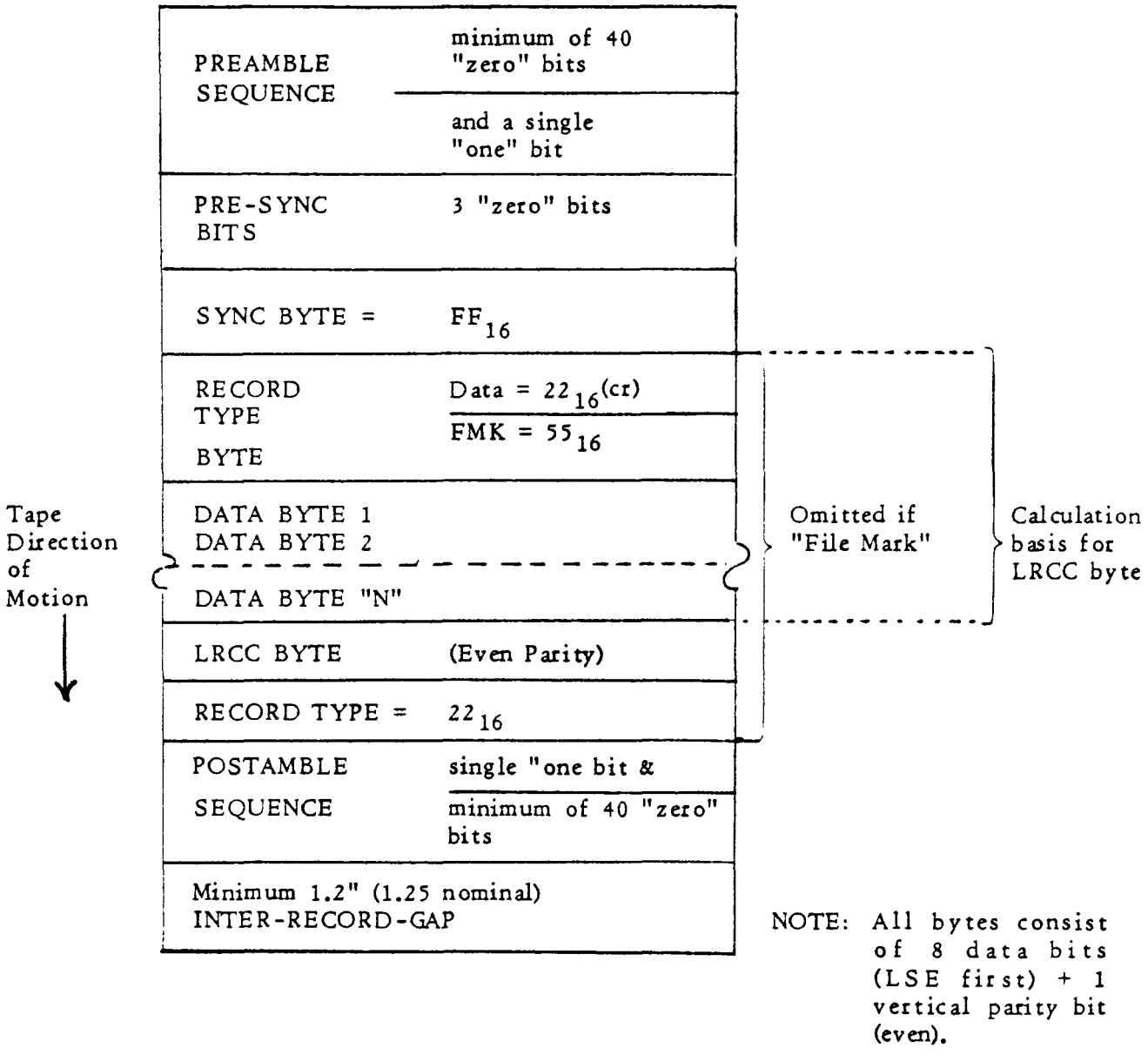


Figure 3-9
Record Format - Cartridge Tape Controller

Cabling

The tape cartridge unit is connected to the computer via a ribbon cable which is attached to the back of the drive, and connected to the controller board which is inserted into the motherboard. The proper orientation of the ribbon cable is shown below.

Figure 3-10
Tape Cartridge Data Cable Orientation

SECTION 4

Memory, Floppy Drive and Winchester Drive Tests

4.0 64K MEMORY TEST PROGRAM

The memory of the 8-bit IMS system is normally found in 64K units. There is one memory board used in the CP/M operating system. The multi-user operating system can have up to 17 64K memory units distributed between all the users.

The program tests an area of memory bounded by the top of the test program and the bottom of the operating system. These bounds are displayed when the program signs on.

To start the program, type **TESTMEMR <cr>**. The following display will appear.

```
TSTMEMR          Rev 1.X

Memory test utility

Beginning address . . . . . 05A9
Ending address . . . . . Dxxx
```

The program will then run through 6 subtests. The terminal will display the current status of the test by printing dots on the screen. The six subtests are:

1. High bit test. This will write an FFH pattern to the memory locations. This will test for a data bit shorted to low.

2. Low bit test. This will write a 00 pattern to the memory locations. This will test for a data bit shorted to high level.

3. Checkerboard bit test 1. This routine will write a 55H pattern (0101 0101) to the memory locations. This will test for a short between data bits.

4. Checkerboard bit test 2. This routine will write an AAH pattern (1010 1010) to the memory locations. This will test for a short between data bits.

5. Walking bit right test. This routine will write a changing pattern to the memory locations. This pattern starts as (1000 0000), then (0100 0000), then (0010 0000), and so on. The high bit walks from left to right. This pattern continues to all the tested locations.

6. Walking bit left test. This routine is similar to test 5 except that the high bit moves from right to left.

ERROR MESSAGES DEVELOPED BY THE MEMORY TEST PROGRAM

The memory test program will report any errors discovered in the operation of the tests. The errors will be reported in the following manner.

Memory error-Address:xxxx Expected value:xx Observed value:xx

The difference between the observed and the expected value will tell you which bit is bad at the indicated address. Since the memory chips are all 1 bit wide, this will also indicate which chip is bad. If errors are displayed, the memory board should be exchanged for another.

4.1 FLOPPY DRIVE TEST

FLOPPY SUBSYSTEM

The floppy subsystem is made up of two units: the floppy controller board which resides in the S-100 bus and the floppy disk drives, which can number up to four in a system. The power is supplied by DC cables which connect to all of the drives and by an AC cable which is used only on the 8" full width drives. The data is transferred by a ribbon cable that connects all of the floppy drives to the controller board.

The 8" drives are available in two different sizes, either full width or half width. The width describes the physical space that the drive takes up in the system. The full width drive is approximately 4.5 inches wide, while the half width is 2.25 inches wide. The full width drives use the AC line voltage to power the spindle motor. The half width drives use 24V DC for the spindle motor. The same test software can be used for both the full and the half width drives. Some specific parmeters can change, however. See Appendix A for more details.

The 8" drives are also available in single or double sided models. The number of sides is determined by the number of read-write heads in the drive. A double sided drive can read both single and double sided diskettes, while a single sided drive can only read single sided diskettes. Disk errors can occur if a double sided diskette is placed in a single sided drive. The diskette label will generally indicate which type of diskette it is.

The 5" drives are also available in full and half width sizes. All of the 5" drives are DC powered. The 5" drives can be either single or double sided. Another option found only on the 5" drives is the availability of quad density format. Density refers to the amount of data that can be contained on the diskette. The 8" floppy drives can read and write in either single or double density, with double density being the norm. The 5" floppy drives can read either single or double density. These drives are known as 48 tpi drives. An available option on the 5" system is a quad drive (also known as 96 tpi drive). This drive will write twice as much data on the diskette as the 48 tpi drive. In running the test software, the type of drive (48 or 96 tpi) must be specified.

THE FLOPPY TEST PROGRAM

To start the floppy drive test, type **TSTF930 <cr>**, and the following menu will appear.

```
IMS International

PROG. ID: TSTF930  Floppy Disk Test Utility  Rev 1.1

**5" Floppies**

For 5", 48 T.P.I. drive(s), type: 1
For 5", 96 T.P.I. drive(s), type: 2

**8" Floppies**

For 8", 48 T.P.I. drive(s), type: 3

?
```

The drive size can be found by looking at the IMS model number. The first digit indicates the size of the drive(s) (5 or 8 inch). The fourth spot indicates the density; a 'Q' indicates a 96 t.p.i. drive and a 'D' is for a 48 t.p.i. drive. (Further details about the IMS model number can be found in Appendix E.)

After the drive size is selected, the following command screen will appear.

COMMAND SCREEN

```
                        IMS International
                   5"  48 T.P.I. Floppy Disk Test

PROG ID:  TSTF930                                          REV 1.0

Drive:  0          Track: ??    Head: 0      Sector: 01

double-density                  SRT: 06      HLT: 004C
N#: 2              EOT: 10      GPL1: 20     DLT: 004C
                   SC: 10       GPL2:        DMA Controller: 8257

Read address:  9900                    Write address:  9900
Free memory:  9900 to 9CFF             Radix: Hex
Soft error(s): 00 00 00 00             FDC base: C0
Hard error(s): 00 00 00 00             Seek verify: ON

Command:
```

DESCRIPTION OF COMMAND SCREEN

Heading: Make sure this matches the type of drives in the system.

PROG ID: Program name and Rev level.

Drive: Currently selected drive

Track: Upon initialization the current track is unknown. The currently selected track will be displayed during test.

Head: Currently selected head

Sector: Currenty selected sector

Density: Currently selected density

N#:	Current value for bytes/sector code (see Command Descriptions)
EOT:	Number of sectors per track
SC:	Number of sectors per track for the format command
SRT:	Drive step rate (see Appendix A for values)
GPL1:	R/W gap length between data field and next ID field
GPL2:	Format gap length between data field and next ID field
HLT:	Head load time in ms.
DTL:	Data length in Read/write table
DMA controller:	defaults to 8257 chip
Read address:	Location in system RAM for disks reads
Write address:	Location in system RAM for disks writes
Free memory:	Available system RAM between top of program and bottom of operating system.
Radix:	Numeric values will be displayed in either decimal or hexadecimal form.
Soft errors:	4 separate error buffers, one for each drive which will save any soft errors found. Drive 0 errors are on the left; then Drive 1,2,3.
Hard errors:	4 separate error buffers, one for each drive which will save any hard errors found. Drive 0 errors are on the left, then Drive 1 errors, Drive 2 errors, etc.
FDC base:	Display base address of controller board, 80H for 8", C0H for 5".
Seek verify:	Determine if track verification is to be performed after a track or recal command.

The following commands are used to test the floppy drive subsystem.

Command		Description
DISKTEST	[all]	DISKTEST will write and verify random data, in all available formats on the selected drive.
DRIVE	[x]	DRIVE will select the currently active drive (0,1,2,3).
EOT	[x]	EOT will set the end of track value.
ERROR	[dr#,S/H,er#] [clear] [abort on/off]	ERROR can be used to view any errors that may have occurred in the running of one of the tests.
HELP		HELP will display the available commands. If the .MSG file was present on the disk, command descriptions are available.
N#	[x]	N# will set the number of bytes per sector in the R/W and format tables. N#=0 for 128 bytes per sector N#=1 for 256 bytes per sector N#=25 for 512 bytes per sector N#=3 for 1024 bytes per sector
QUIT		QUIT will exit a program and perform a warm start.
SRT	[x]	SRT will select the step rate for the drives. See Appendix A for correct values.
VERIFY		VERIFY is used to check the formatting on a diskette.

To thoroughly test your floppy disk drives, follow this procedure:

1. Insert a scratch diskette (one with no important data) into the drive.

2. Set the step rate to the proper value (found in Appendix A) by typing **SRT value <cr>.**

3. Type **DISKTEST ALL <cr>** and press any key to start the test.

4. N# will increment. Stop the test by pressing the Escape key after N# has gone past 3 and returned to 0.

5. Check the error count. Look at the part of the command screen that looks like this:

```
Soft Errors:    00 00 00 00
Hard Errors:    00 00 00 00
```

The leftmost pairs of digits hold the soft and hard error counts for drive 0; the next set is for drive 1,etc. If these locations are all equal to zero after the test, there are no floppy drive errors. If there are errors on only one drive, see if the scratch diskette is bad by repeating the test with that diskette in another drive. If there is no problem with the scratch diskette, there is probably a hardware error.

The key to determining the fault in the floppy subsystem is to correctly interpret the error messages. The errors can be viewed by typing **E drv# S/H**, where drv# stands for the drive that the errors occur on, and S/H is S for soft errors and H for hard errors. The error message will give a description of the error and a possible cause.

A. Errors Developed in Disktest - POSSIBLE CAUSES

(1) SRT has not been set to correct value. (See Appendix A.) **(2)** Incorrect power is being supplied to the drives. (See Appendix A.) **(3)** Loose or bad power or data cabling. **(4)** Bad diskette placed in drive. Replace diskette. **(5)** If errors occur on only one drive, switch diskettes between drives. **(6)** If errors occur on only one drive, possible bad drive. **(7)** If errors occur on both drives, possible bad controller.

4.2 WINCHESTER DRIVE TEST

WINCHESTER SUBSYSTEM

The Winchester subsystem is made up of three main units, those being the Winchester controller card, which resides in the S-100 bus, the interface card, which plugs onto the back of the drive, and the drive itself. The power is supplied by a DC cable and by an AC cable for the 8" drives. The data is transferred by a ribbon cable that connects between the controller card and the interface card.

The data is held on the drive in 512 byte sectors. There are a number of sectors per track. The track specifies a head and a cylinder location. The drives can have as many as eight heads and 512 cylinders. This would give a total of 4096 tracks. The error message given by the operating system defines the bad location in terms of a track and a sector location.

Start the Winchester test by typing **TSTW <cr>**. The system will respond with the following message:

```
PROG ID:  TSTW      Winchester Test Utility

**5" Winchesters**

For   5   megabyte drive,        type:   1
For   6   megabyte drive,        type:   2
For   7   megabyte drive,        type:   3
For  11   megabyte drive,        type:   4
For  12   megabyte drive,        type:   5
For  15   megabyte drive,        type:   6
For  24   megabyte drive,        type:   7


**8" Winchesters**

For  10   megabyte drive,        type:   8
For  20   megabyte drive,        type:   9
For  40   megabyte drive,        type:  10
For  80   megabyte drive,        type:  11

?
```

Type the number that corresponds to the size of the drive to be tested, followed by a carriage return. The test program will then initialize the drive and display the command screen.

TEST PROGRAM COMMAND SCREEN

```
                    8 " W I N C H E S T E R   D R I V E   S T A T U S

Unit:  0        Head:  0        Cylinder:  0        Sector:  0          Status:  10

PROG ID:  TSTW                                                  REVISION 1.X

Read address:  6900                          Write address:  6900

Format byte:  E5                             Seek verify:  ON

Free memory:  6900 to xxxx Drive capacity:  40 megabytes

Error counter:  0       ON


Command:
```

DESCRIPTION OF THE COMMAND SCREEN

The command screen will display the current active location. **Unit** describes the active drive, normally 0, although this number can range up to 3 on systems tht contain multiple Winchesters. **Head** describes the current active head. This value can range from 0 to 7 on the various Winchester drives (see Appendix B for drive information). **Cylinder** shows the currently selected cylinder location. **Sector** shows the currently selected sector location. The **Status** byte gives information regarding the current controller status (see Appendix B for information on the status byte).

The address information given defines the location in system RAM where the data transfer is to take place. The **Read address** is where the sector data being read is transferred to. The **Write address** is the source of the data that is written to the sector. The **Free memory** lists the available RAM locations above the program and includes the read/write address.

The **Format byte** dislays the current byte being used for the format and the verify commands. It defaults to E5H which is the normal format byte used on all of the drives. **Seek verify** can be enabled or disabled by the user by using the SEEKVER command. Normally, it is on. When it is on, the controller will verify the current location with the header on the sector. If there is not a match, an error is generated and the seek would be aborted. The **Drive capacity** is displayed to enable the user to verify that the correct choice was made during initialization. The **Error counter** will keep a running count of any errors found during execution of the program. This area will be explored in the next section.

COMMANDS USED

CYLINDER	UNIT	QUIT	ERROR
READ	VERIFY	SEEKVER	HELP
SECTOR	HEAD	WRITE*	FORMAT*

*** - DESTRUCTIVE**

The commands listed above are of two distinct types, destructive and non-destructive. Care must be taken when using this program so that you do not destroy customer data areas if it is unnecessary to do so. The destructive commands are to be used only if there is no way to save the customer's data. The destructive commands are shown with an asterisk (*) in the above list.

One of the most useful commands for the novice user of this program is the **HELP** command. Contained within the program are descriptions of all of the commands. Typing **HELP** will display all of these commands. You can then type the command that you are interested in to view an explanation and syntax of the command in question.

COMMAND DESCRIPTION

The commands will now be discused in more detail with the required syntax, and the normal use of the commands. Those that are considered **destructive** will be preceded with an asterisk (*).

NOTE: COMMANDS PRECEDED WITH AN ASTERISK (*) ARE DESTRUCTIVE!

Command		Description
CYLINDER	[cylinder number]	CYLINDER is used to set the current cylinder position on the Winchester drive.
ERROR	[error number] [clear] [abort]	ERROR is used to examine errors that were recorded into the error buffer.
*FORMAT	[byte]	FORMAT will format the entire disk. It cannot be used to ready the drive for an operating system.
HEAD	[head number]	HEAD is used to set the current head on the drive.
HELP		HELP can be used to view a description of any available command.

QUIT		QUIT will perform a warm start.
READ	[loop] [count]	READ will read in the current sector to the read buffer.
SECTOR	[sector number]	SECTOR is used to set the currently active sector.
SEEKVER	[on] [off]	SEEKVER is used to enable or disable seek verification.
UNIT	[unit number]	UNIT is used to set the unit to be tested.
VERIFY	[byte]	VERIFY will read each sector on the currently selected drive.
VERIFY HEADER		VERIFY HEADER will examine the headers and the ECC code on each sector of the drive.
*WRITE	[loop]	WRITE will write the data from the write buffer to the currently selected sector.

A good non-destructive winchester test is done by typing **VERIFY HEADER <cr>**. The test will last about 15 minutes. Afterwards, check the error counter. If it is zero, there are no errors and you can type **QUIT <cr>** to end the test. If there are errors, follow the steps indicated in part B of the Error Messages section.

ERROR MESSAGES

The following is a list of all the error messages developed by the program. Included is an explanation of the error and possible causes.

Winchester is Not Selected

The controller card is unable to select the drive. This could be a fault on the controller, the drive, the cabling or the power supply.

Error Attempting to Reset Drive

The drive was selected and ready. In attempting to do a recalibration, the Trk 0 signal was not observed. This could be due to the drive actuator being locked.

NOTE: Each of the above error conditions gives the user the option of continuing the test. The message **DRIVE NOT INITIALIZED** will appear on the command screen. The test should be discontinued if this message appears.

Unit is Not Ready

During the running of the test the ready signal from the controller was lost. This could be a fault on the controller board.

Drive is Not Ready

The test program attempted to select a drive, but the drive did not respond with a ready signal. Make sure a valid drive was selected and that it has the proper cable connections.

Drive Write Fault Received

A write fault was received from the Winchester drive during a write. This fault is developed by the drive.

No Interrupt Received From Operation

An interrupt signal must be developed by the controller during normal operation. Check controller card and shunting.

Unit Cannot be Selected

The controller status byte does not contain an active select bit. This fault can reside on the controller, interface or drive.

ECC-Uncorrectable Hard Error

ECC error detected by the controller. The error was larger than 8 bits long, and the data was still unreadable after 5 retries.

ECC-Correctable Hard Error

ECC error detected by the controller. The error was 8 bits or less in length, and the data was still unreadable after 5 retries.

ECC-Uncorrectable Soft Error

ECC error detected by the controller. The error was larger than 8 bits long, and the data was readable before 5 retries were completed.

ECC-Correctable Soft Error

ECC error detected by the controller. The error was 8 bits or less in length, and the data was readable before 5 retries were completed.

9-Bit Pattern was Corrected

The ECC circuitry will repair any data failure up to 8 bits in length. If a 9 bit pattern was corrected, this would indicate a failure on the controller board.

Header Verification

The information read in the header area of the requested sector did not match the requested location. This could be due to data corruption on the drive, a writing problem on the controller, or a reading problem on the controller board.

Disktest Buffer Verification

The data in the buffer did not match the format byte. This error is developed by the **VERIFY** command. This command expects all data areas to contain the format byte, and this error would be developed if that command is run on a customer's drive that contains data.

A. Command Screen not Displayed - POSSIBLE CAUSES

1. Test is being run in a multi-user operating system.
2. Incorrect power is being supplied to the drive or interface card. See Appendix A.
3. Loose or bad power or data cabling.
4. Bad controller board (replace first).
5. Bad interface board (replace second).
6. Bad Winchester drive (replace third).

There are a number of conditions to be met before the TSTW command screen will be displayed. The test program will look for a ready drive. The drive must be up to the correct operating speed before it will become ready. Check the cables going to the drive. Make sure both the power connections and the data connections are tight.

When the system is powered up, listen to the drive motor. You should hear the platter coming up to correct speed. The drive may be bad if the platter is not turning with correct power going to the drive. On the 8" Winchesters make sure that the platter and the head actuator are unlocked.

The drive must present a ready signal to the controller bord. This signal must be sent to the controller board by the interface board. A bad interface card or bad data cable would keep this signal from being transferred.

The second condition that needs to be met to enter the command screen mode is a selected drive. A problem in this area could be due to a fault on the logic card on the drive, or a bad interface or controller board.

B. Errors Developed in Running 'VERIFY HDR' Command

Error Interpretation

The most common errors developed by the VERIFY HDR command are ECC type of errors. ECC stands for error correcting code, which is used on the Winchester controller board to locate and possibly correct bad data in the sector. If the error is larger than 8 bits, then the operating system will report the error to the user as a Read error. The test program will flag these errors as Uncorrectable ECC Errors. Depending on the number of errors reported, various repair methods are available.

A small quantity of errors can possibly be repaired by using the test program. The procedure is to first write down the bad locations found by the VERIFY HDR command on a sheet of paper. The errors can be viewed by typing **ERROR** while at the command screen. The first error will be displayed. The next error can be viewed by typing **<cr>**. Continue to type **<cr>** until all of the errors are viewed, then type **cr** to return to the command screen. Go to the first location by using the HEAD, CYLINDER and SECTOR commands. Read the sector into the buffer by typing **READ.** The error counter should increment. Write the data back out to the sector by typing **WRITE.** Read the location again. If the error counter does not increment, then the header is now correct and the ECC agrees with the data in the sector. Repeat the procedure for all of the bad locations. When completed, clear the error butter with the command **ERROR CLEAR.** Rerun the **VERIFY HDR** command. The error counter should now report 0 errors. If any of the errors return, the error cannot be repaired and must be locked out by either the FMTW program or the WALT program located on the operating system disk.

APPENDIX A - FLOPPY DISK SUBSYSTEM SPECIFICATIONS

FLOPPY DISK SPECIFICATIONS

Physical Size	Number of Sides	Data Capacity	SRT	Manufacturer
8" full	1	610 kbytes	8	Shugart 801
8" full	2	1220 kbytes	3	Qume 842
8" half	2	1220 kbytes	4	Qume 242
5" half 96 tpi	2	772 kbytes	6	Teac FD-55F
5" half 48 tpi	2	386 kbytes	6	Teac FD-55B

FORMAT SPECIFICATIONS

Physical Size	Operating System	Number of Tracks	Number of Reserved Tracks	Sector Size
8" all	CP/M	77	2	256 bytes
8" all	TurboDOS	77	0	1024 bytes
5" 48 tpi	CP/M	40	2	256 bytes
5" 48 tpi	TurboDOS	40	0	1024 bytes
5" 96 tpi	CP/M	80	2	256 bytes
5" 96 tpi	TurboDOS	80	2	1024 bytes

Physical Size	Operating System	Density	N#	SC	EOT
8" all	CP/M	single *	0	1A	1A
8" all	CP/M	double	1	1A	1A
8" all	TurboDOS	double	3	08	08
5" all	CP/M	double	1	10	10
5" all	TurboDOS	double	3	05	05

*Single density is normally not used as an IMS format; however, many different software packages are distributed in IBM single density 8" format (IBM 3740) and the 8" IMS systems will read this format.

FLOPPY POWER REQUIREMENTS

SIZE	115V AC	+24V	+12V	+5V	-16V	0V
8" full	Yes	Yes	No	Yes	Yes	Yes
8" half	No	Yes	No	Yes	No	Yes
5" all	No	No	Yes	Yes	No	Yes

APPENDIX B - IMS SYSTEM INFORMATION

All model numbers are expressed as [EEB-nWWW-xFFz] where

EE = basic system enclosure

[5X]	=	MODEL 5000SX TABLE TOP SYSTEM
[5I]	=	MODEL 5000IS INTEGRATED SYSTEM
[8X]	=	MODEL 8000SX
[8S]	=	MODEL 8000S

B = 8 or 16 bit option (Most are 8 bit)

n = number of Winchesters (omitted if n=0 or n=1)

WWW = type of Winchesters (omitted if none)

[W6]	=	5" 6	Mb
[W12]	=	5" 12	Mb
[W24]	=	5" 24	Mb
[M6]	=	8" 6	Mb
[M12]	=	8" 12	Mb
[M24]	=	8" 24	Mb
[M40]	=	8" 40	Mb
[M85]	=	8" 85	Mb

x = number of floppy drives

FF = type of floppy drive

[DH]	= 5"	double sided half width	48 tpi
[QH]	= 5"	double sided quad density half width	96 tpi
[DH]	= 8"	double sided half width	48 tpi

IMS SYSTEM VERSIONS

BOARDS USED

System	CPU	I/O	Memory
A	451	44x	465
B	645	631	465
C	645	480	465
D	971		465

BOARD DESCRIPTIONS

Name	Number	Description
CPU-A	451	Z-80 Processor Board
CPU-B	645	Z-80 Processor Board
CPU-IO	971	Z-80 Processor Board
64K DRAM	465	Memory
256K DRAM	961	Memory
SPIO-A	444	Input/Output (2 serial ports, 1 parallel port)
SPIO-B	631	Input/Output (2 serial parts, 1 parallel port)
4SIO	480	Input/Output (4 serial ports)
MPU	740	Multiprocessor Unit
MPU	861	Multiprocessor Unit
FDC	931	Floppy Disk Drive Controller
WDC	820	Winchester Drive Controller